FINAL REPORT

FOR

OPTIMUM CHARGING SYSTEM STUDY PROGRAM

CONTRACT NO. NAS5-3785

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TABLE OF CONTENTS

ABSTRACT

This report summarizes in detail the complete study program for the design, development and performance of an Optimum Charging System as required in NASA Contract No. NAS5-3785.

A primary study program contract and an "add-on" contract were awarded to Engineered Magnetics by NASA.

Under the provisions of the primary contract, two Ampere-Hour Meter Taper Charge System breadboards were designed, fabricated and tested: one breadboard was submitted for use to NASA and the other was retained for use at Engineered Magnetics. These breadboards use an Ampere-Hour Meter as the controlling device to charge nickel-cadmium batteries. A Solar Array Simulator was also developed to simulate the actual Solar Array for test functions at Engineered Magnetics.

The "add-on" contract authorized the design, fabrication and testing of an Adhydrode-Optimum Tracking System breadboard which utilizes the Adhydrode Voltages of the Adhydrode Battery Cells for the charge controlling factor in lieu of the Ampere-Hour Meter controlling device. The Adhydrode-Optimum Tracking System contains a Maximum Power Tracker circuit to attain optimum power transference to the battery.

The Ampere-Hour Meter Taper Charge System was modified to serve as a back-up to the Adhydrode-Optimum Tracking System and simultaneously furnishes a signal that can be converted to ampere-hours with calibration curves. Either the Ampere-Hour Meter controlled breadboard or the Adhydrode Voltage controlled breadboard can be operated as a separate self-contained charge control system.

In addition, considerable testing and experimenting was conducted on the Gulton 6 Ampere-Hour Adhydrode cells for evaluation purposes.

I. BASIC DESIGNS

A. AMPERE-HOUR METER TAPER CHARGE SYSTEM

1. Block Diagram

a. The engineering study of the primary contract began on April 10, 1964. The main objective was to design an Optimum Charging System which uses an Ampere-Hour Meter as the controlling device to charge nickel-cadmium batteries. The engineering study determined that the basic Ampere-Hour Meter Taper Charge System should be comprised of five major sections as follows (see Figure 1-1, Block Diagram):

b. A Charge Control Regulator which charges the battery by three different modes in each charge cycle. Initially, the battery is charged in a solar array limited mode; then switched to a constant voltage taper charge as the battery voltage rises; and then finally switched to a lower voltage trickle charge after the battery is fully charged.

c. An Analog-to-Digital Converter which converts the analog signal (battery current as monitored across the shunt) to a digital, or frequency signal. Five coulombs (five ampere-seconds) to equal one pulse at the input to the Frequency Divider (Countdown).

d. A Memory which stores information related to the state of battery charge during both the charge and discharge modes.

e. Charge Mode Logic Circuits to provide signals to the Charge Control Regulator for switch-to-trickle charge mode; to the Analog-To-Digital Converter for provision of a unidirectional output for a bi-directional input; and to the

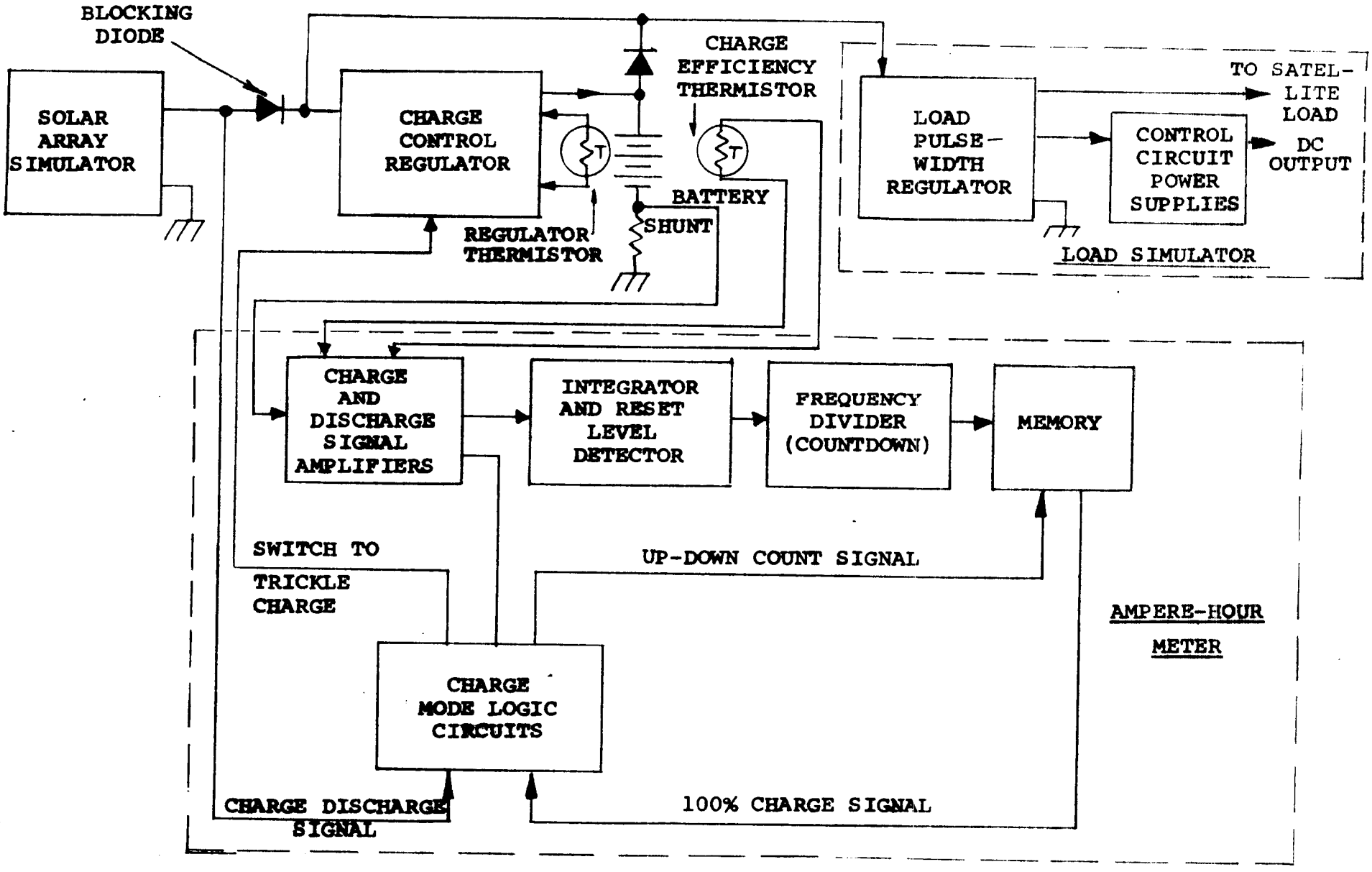


FIGURE 1-1. AMPERE-HOUR METER TAPER CHARGE SYSTEM, BLOCK DIAGRAM.

Memory to control the direction of counting.

f. In addition to the Ampere-Hour Meter Taper Charge System, a Load Simulator was fabricated to provide loads on the battery and the solar array to simulate the satellite electrical loads. A Load Pulse Width Regulator was also fabricated to be used in conjunction with the Load Simulator to provide high efficiency conversion.

The basic system was breadboarded for evaluation of performance.

2. Performance Characteristics

a. Some performance characteristics of the Ampere-Hour Meter Taper Charge System are as follows:

(1) The efficiency of the battery Charge Control Regulator is between 93 and 94 percent.

(2) The linearity of the Analog-To-Digital Ampere-Hour Meter control circuit is better than one percent.

(3) Power drain in the Analog-To-Digital Ampere-Hour Meter control circuit is less than one watt.

B. ADHYDRODE-OPTIMUM TRACKING SYSTEM

1. Block Diagram

a. Engineered Magnetics was awarded an "add on" contract to the Optimum Charging System study program by NASA which became effective on June 24, 1965. The main objective was to design, fabricate, and test an Optimum Charging System breadboard which would use the Adhydrode voltages of Gulton 6 Ampere-Hour cells as the charge control device instead of the Ampere-Hour Meter. This system incorporates a circuit designated as the "Maximum Power Tracker." The Maximum Power Tracker circuit

accomplishes maximum power transference from the Solar Array to the Battery. The previously designed Ampere-Hour Meter Taper Charge System was modified to serve as a backup for the Adhydrode-Optimum Tracking System and, also, to simultaneously furnish a signal that can be converted into ampere-hours with calibration curves. The block diagram of the Adhydrode-Optimum Tracking System is shown in Figure 1-2.

b. An explanation of the basic design follows:

(1) Maximum power transference from the Solar Array to the Battery is accomplished by changing the duty cycle of the Pulse-Width Modulated Transistor Switch by means of a feedback signal. Changing the duty cycle effectively changes the load line in terms of impedance.

(2) When the feedback loop of the system is closed, the duty cycle of the Transistor Switch will adjust in such a manner as to intersect with the point of maximum power on the Solar Array voltage/current curve (see Figure 1-3).

(3) The duty cycle of the Transistor Switch is altered by signals from the Perturbing Signal Source which momentarily shifts the load line.

(4) Depending on the position of the load line, positive or negative going Sense Signals appear at the load (Battery). A negative going Sense Signal energizes Phase Detector A through the Inverting Amplifier and a positive going Sense Signal energizes

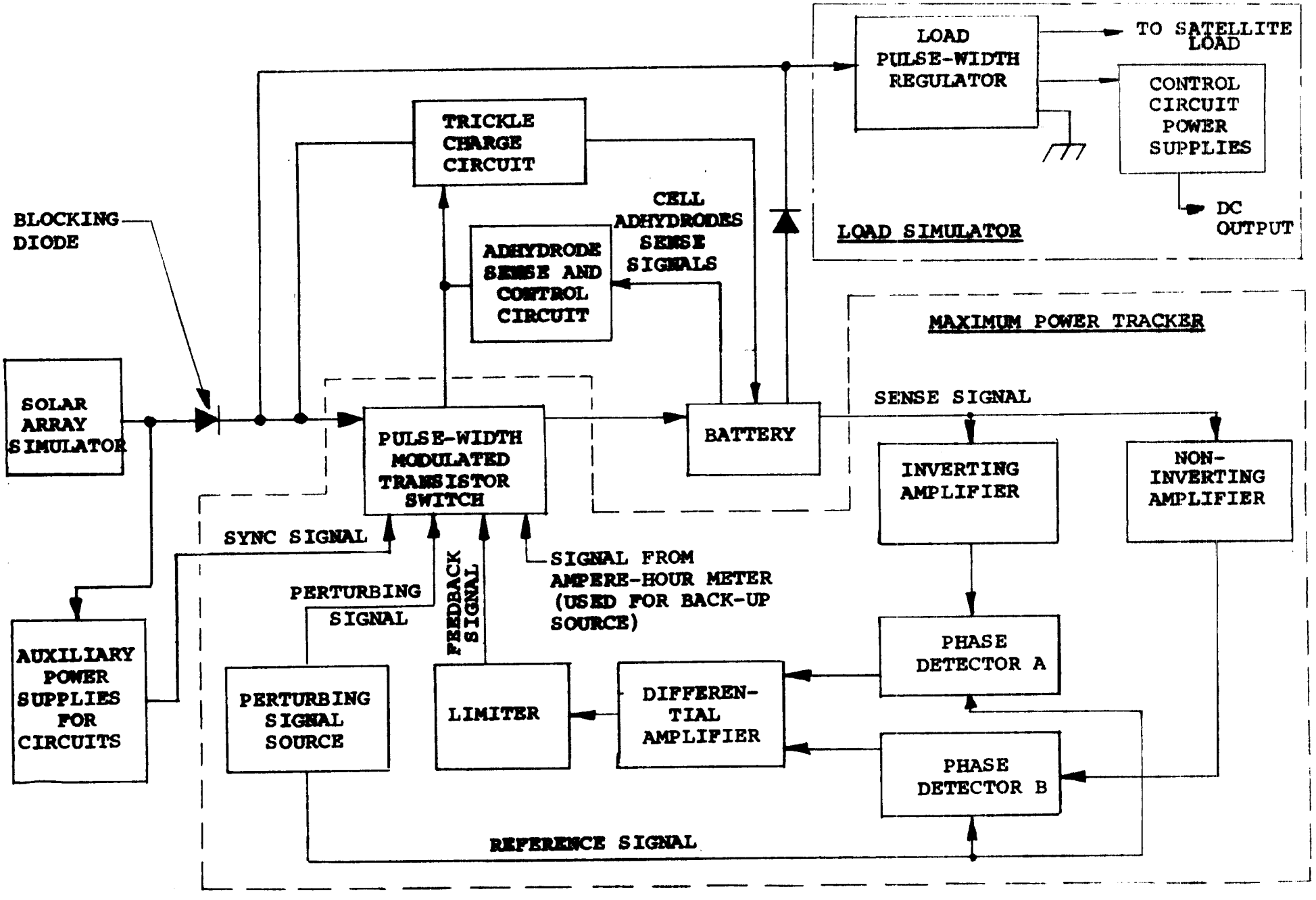


FIGURE 1-2. ADHYDRODE-OPTIMUM TRACKING SYSTEM BLOCK DIAGRAM.

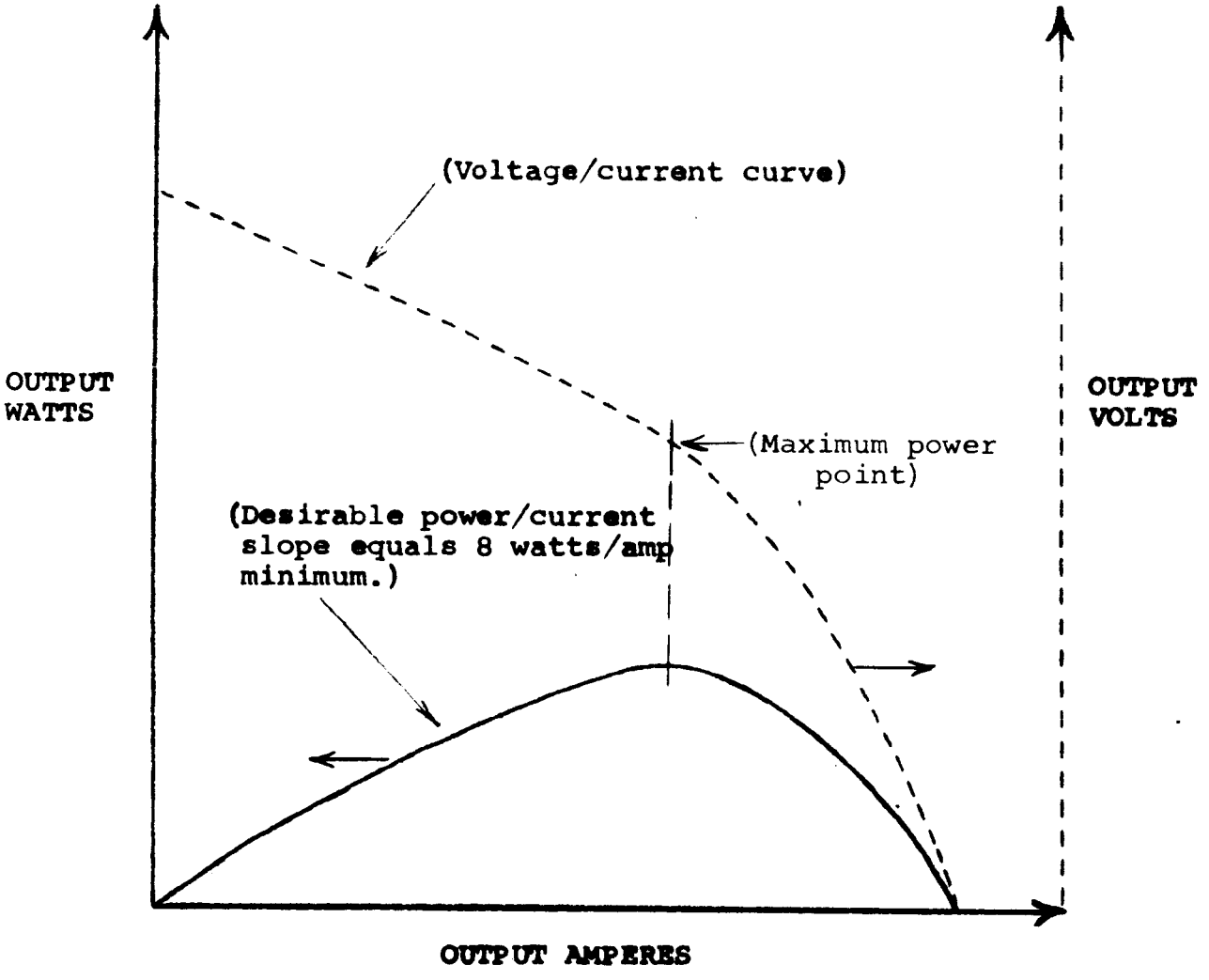


FIGURE 1-3. MAXIMUM POWER CHARACTERISTICS OF SOLAR ARRAY INPUT POWER TO ADHYDRODE-OPTIMUM TRACKING SYSTEM.

Phase Detector B through the Non-Inverting Amplifier.

(5) According to which Phase Detector is energized, the Differential Amplifier output will swing in such a direction through the Limiter as to decrease or increase the duty cycle of the Transistor Switch so that the load line will always shift toward the point of maximum power on the Solar Array voltage/current curve.

(6) When the Adhydrode voltage (or voltages) of the Battery reaches a predetermined level the Adhydrode Sense and Control Circuit generates a signal which shuts off the Pulse Width Modulated Transistor Switch and energizes the constant current Trickle Charge Circuit. Trickle charge current is determined by the setting of a power potentiometer (R1, see Schematic 57854) installed on the breadboard.

(7) The Adhydrode Sense and Control Circuit, as designed, is capable of receiving signals from 1 to 4 Adhydrode cells. The charger will switch to trickle charge upon receiving a signal from either the Adhydrode Sense and Control Circuit or from an external backup source, such as the Ampere-Hour Meter.

(8) The Auxiliary Power Supplies receive their input directly from the Solar Array output (at the point just before the Blocking Diode) and furnish power to the Maximum Power Tracker, Trickle Charge Circuit, and Adhydrode Sense and Control Circuit. Due to the Blocking Diode, the Auxiliary Power

Supplies are inoperative during the battery discharge cycle.

2. Performance Characteristics

a. The performance characteristics of the bread-board design of the Adhydrode-Optimum Tracking System are as follows:

(1) The system will respond with reasonable speed (in the order of several seconds) if the slope of the power output versus current output characteristic of the input power source is higher than 8 watts per amp (see Figure 1-3).

(2) The system will function satisfactorily if the resistance of the output load (internal resistance of the battery) is more than a few tenths of an ohm.

(3) The low frequency ripple amplitude at the input power source can be held well below one volt peak-to-peak for typical input power and output load characteristics.

(4) The response time of the system to output load variations, source variations, or changes from discharge to charge is typically about several seconds.

(5) The error factor of the system is about 4%, excluding the power dissipation of the Transistor Switch.

(6) The power dissipation of the system is less than 500 MW, excluding the power dissipation of the Transistor Switch.

C. OPTIMUM CHARGING SYSTEM DESCRIPTION

The Optimum Charging System has 6 modes of operation to charge the Battery as indicated in Figure 1-4.

1. Maximum Power Charging controlled by Ampere-Hour Meter.

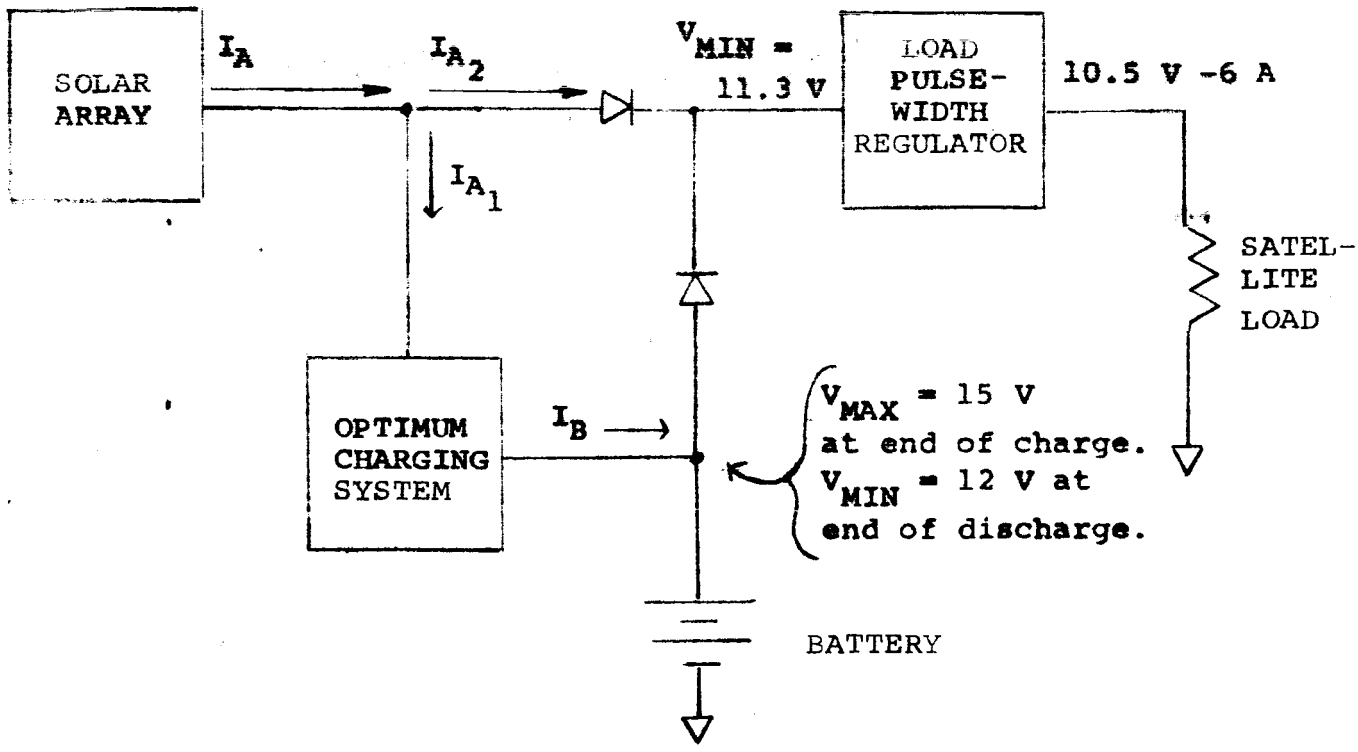


FIGURE 1-4. OPTIMUM CHARGING SYSTEM OPERATING CONDITIONS.

2. Maximum Power Charging controlled by Adhydrode Voltage.
3. Maximum Power Charging controlled by either the Ampere-Hour Meter or the Adhydrode Voltage.
4. Taper Charging controlled by Ampere-Hour Meter.
5. Taper Charging controlled by Adhydrode Voltage.
6. Taper Charging controlled by either the Ampere-Hour Meter or the Adhydrode Voltage.

During the light period, the Solar Array supplies power to the Satellite Load and to the Optimum Charging System which keeps the Battery charged. During the dark period the Battery, charged by the Optimum Charging System, supplies power to the Satellite Load.

The Ampere-Hour Meter controlled Optimum Charging System or the Adhydrode Voltage controlled Optimum Charging System can be operated separately or in conjunction with each other. When operating together, either controlling signal (Adhydrode Voltage or Ampere-Hour Meter) can initiate charging the Battery depending on which controlling signal comes first. The control signal can be set to occur at a designated time. The Optimum Charging System is efficiently used as an Adhydrode Voltage controlled system with the Ampere-Hour Meter as the back-up control signal.

Both Optimum Charging Systems were designed and fabricated having the following operating conditions:

(1) Load Pulse Width Regulator Efficiency	94%
(2) Load 10.5 V at 6 A	63 watts
(3) Number of Battery Cells	10
(4) Dark Period (discharge)	30 mins.
(5) Light Period (charge)	60 mins.
(6) V_{MIN} Solar Array (end of charge)	15.6 V

(7) Solar Array Voltage vs. Time	See Fig. 1-5, Curve (A)
(8) Battery Voltage vs. Time	See Fig. 1-5, Curve (B)

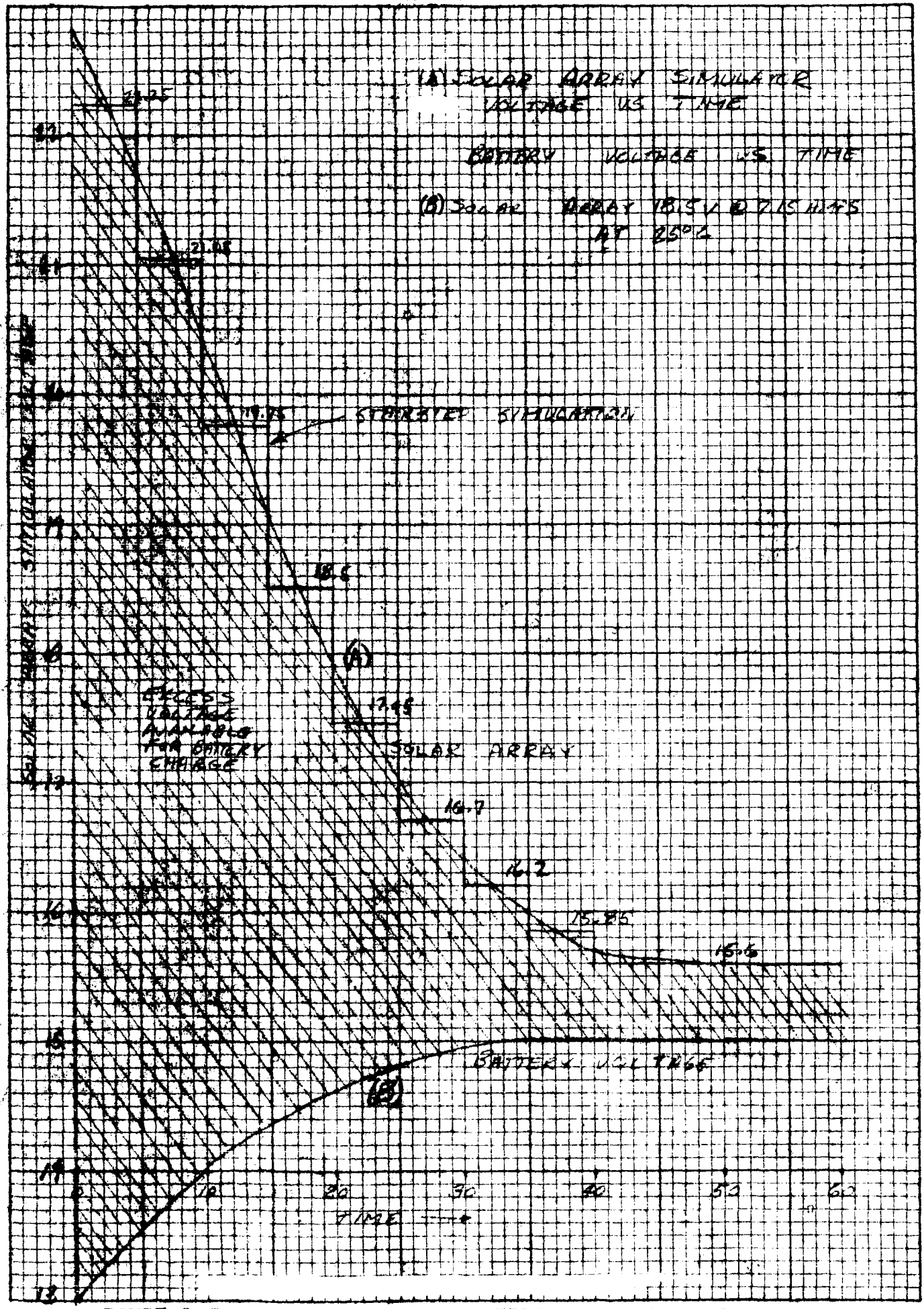


FIGURE 1-5. SOLAR ARRAY AND BATTERY VOLTAGE VERSUS TIME.

II. DETAILED CIRCUIT DESCRIPTION

A. CHARGE CONTROL REGULATOR (PART OF AMPERE-HOUR METER TAPER CHARGE SYSTEM, SEE SCHEMATIC 59055.)

1. Operation

a. The Charge Control Regulator is a switching type regulator with approximately 94% efficiency. The block diagram, Figure 2-1, shows the six functional elements of the Charge Control Regulator. Regulation is accomplished in a manner similar to that of a servo amplifier, in that an error or difference voltage is used to control the output and thereby minimize the error. The voltage difference between the Reference Voltage (CR106) and a sample of the regulated output is detected and amplified by the Differential Amplifier (Q108, Q109). The Level Detecting Amplifier (Q106, Q107) senses the magnitude of the error signal and varies the duty cycle of the Switching Transistor Q103 (on-time to off-time) in a direction to correct any deviation from the preset voltage.

b. The Differential Amplifier takes a true sample of the output voltage to compare with the constant Reference Voltage. A resistance divider, R116 and R117, across the regulated output is used to provide this sample. The Level Detecting Amplifier is synchronized by the converter in the Control Circuit Power Supplies section. High frequencies are used to accelerate the response time of the system for faster correction of output voltage changes.

c. By varying the timing of pulses to the base of Switching Transistor Q103, the transistor can be switched on and off with a varying duty cycle. This is shown in Figure 2-2. When the

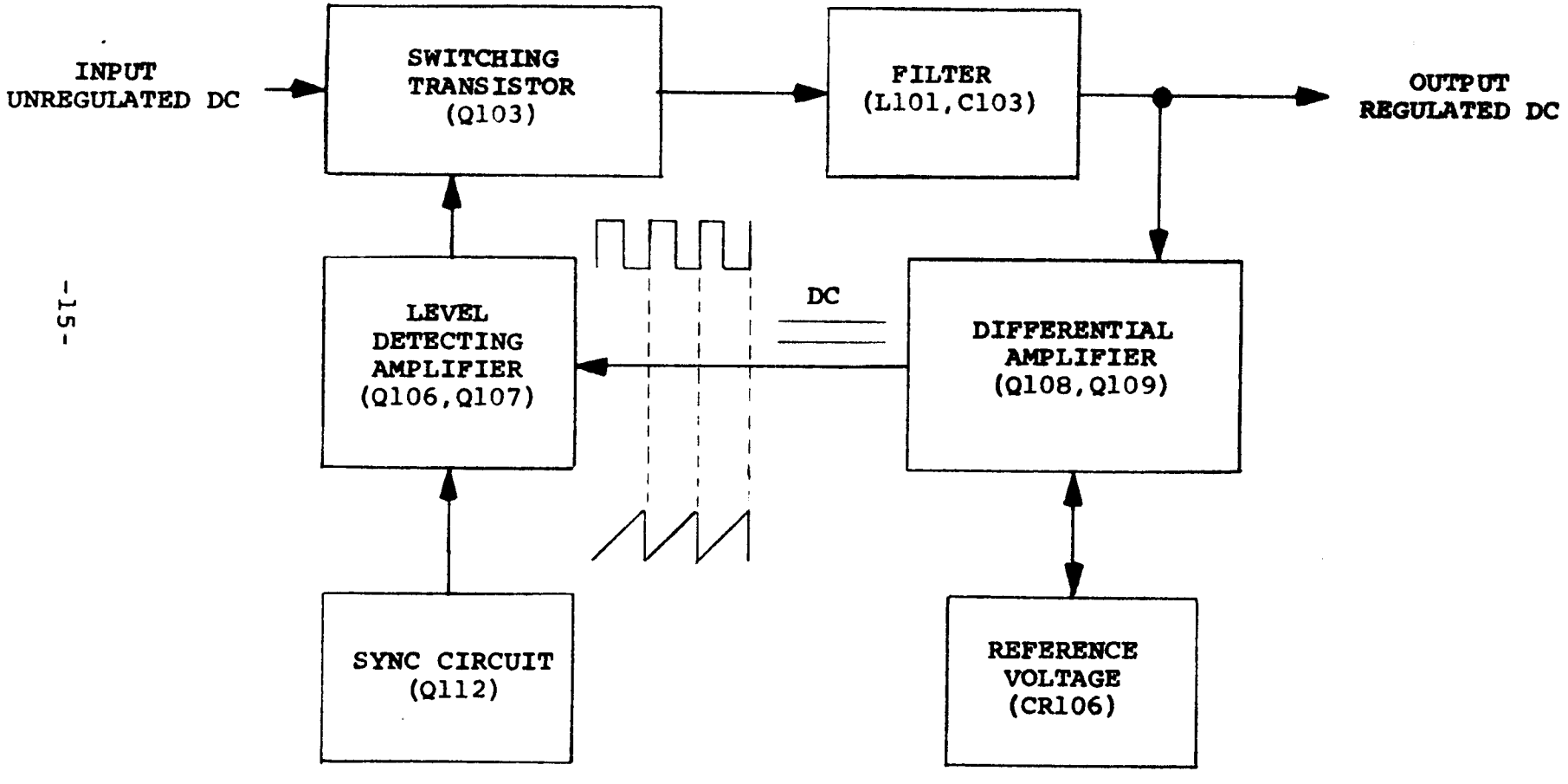


FIGURE 2-1. CHARGE CONTROL REGULATOR BLOCK DIAGRAM.

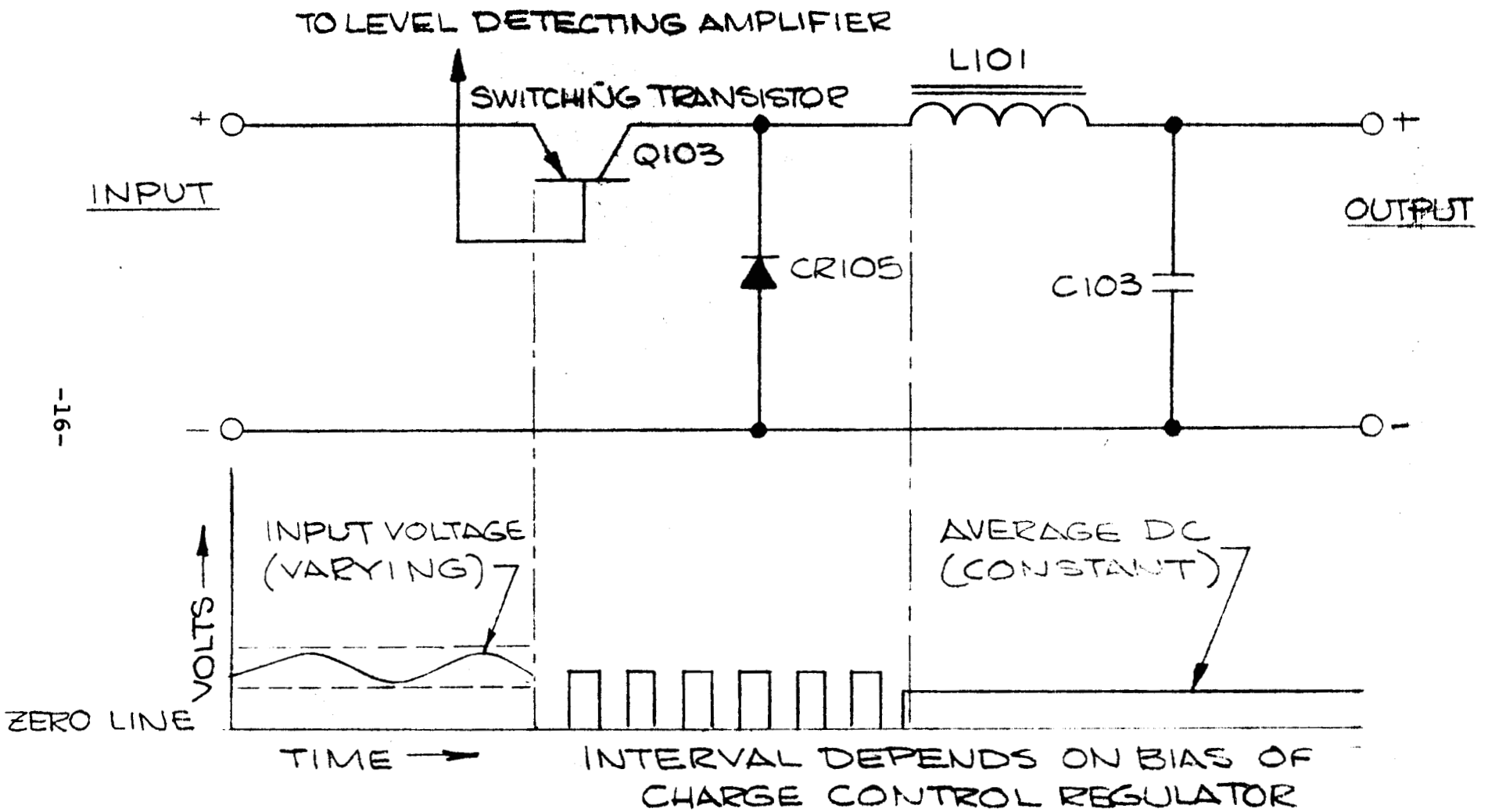


FIGURE 2-2. SWITCHING TRANSISTOR AND FILTER.

Transistor Switch is on, the losses are a function of the transistor saturation resistance which is extremely low. During the Transistor Switch off period no losses are sustained. Efficiency and power handling capability are very high.

d. A filter circuit, L101 and C103, follows the Switching Transistor to average the pulsed output. A typical sequence of events can be followed to demonstrate circuit performance. If the output regulated voltage tends to rise, the Differential Amplifier will sense this increase. This increase in output voltage will be compared to the constant Reference Voltage and result in an error signal. The error signal is fed back to the Level Detecting Amplifier, which reduces the time duration of the drive pulse output. Since drive to the base of the Switching Transistor is shorter in time duration, the on-time becomes shorter. The filtered output of pulses from the Switching Transistor will result in a lower average regulated and corrected output voltage.

e. The purpose of the Sync Circuit is to ensure that the Charge Control Regulator does switch at the same frequency as the Control Circuit Power Supply. This avoids the possibility of beat frequencies between various parts of the system. Q112 performs this sync function. Q112, C105 and R122 make up a ramp generator. Each time a pulse appears at the base of Q112, Q112 saturates momentarily which discharges C105. In between discharge pulses, C105 charges through R122.

2. Input-Output Equation

a. In the simplified schematic of Figure 2-2, if no losses are assumed for Transistor Switch Q103 and Choke L101 then,

Output Voltage = Input Voltage X Duty Cycle of the Switching Transistor Q103

Duty Cycle is defined to be $\frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T}$

where T is the period of the chopping frequency of Q103.

3. Design Parameters

a. If the Charge Control Regulator is visualized as a feedback amplifier, then the required regulation to maintain the charging voltage as the input (Solar Array) and load (Battery) varies is governed by the open loop gain. This is shown in Figure 2-3.

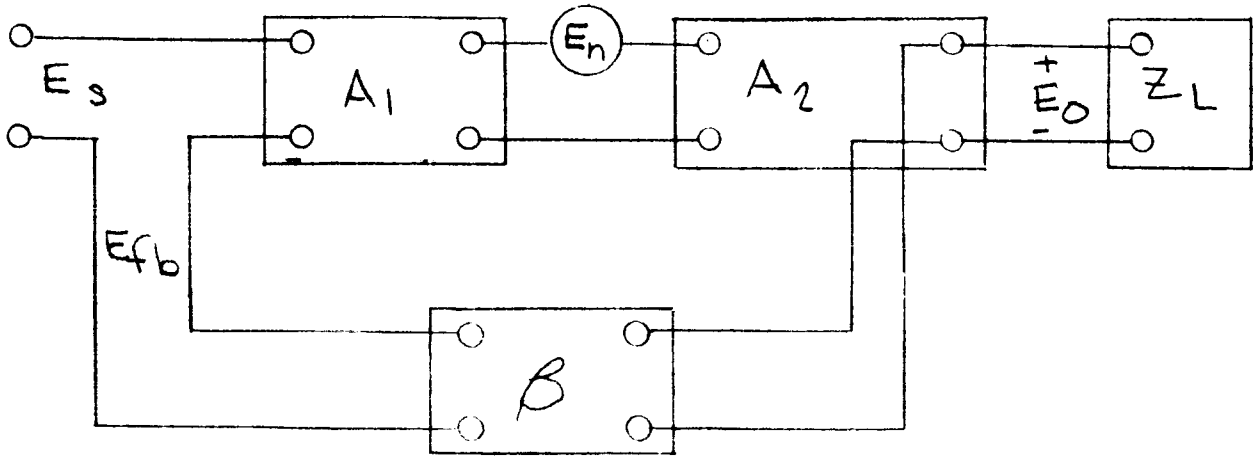


FIGURE 2-3. CHARGE CONTROL REGULATOR IN TERMS OF FEEDBACK AMPLIFIER CONFIGURATION.

b. Employing the following equations,

$$E_o = \frac{A}{1-A\beta} E_s + \frac{1}{1-A\beta} E_n$$

$$Z_o = \frac{1-(A\beta)\ \text{short circuit}}{1-(A\beta)\ \text{open circuit}}$$

where: $A = A_1 \times A_2$

Z_o = output impedance with feedback

Z = output impedance with feedback ineffective

E_o = output variation

E_n = noise (Array voltage variation)

E_s = reference voltage

Applying the equations,

$$E_o = \frac{1}{1-A\beta} E_n$$

$$Z_o = \frac{Z}{1-(A\beta)\ \text{open loop}}$$

$E_s = 0$ in terms of AC variation

$(A\beta)_{\text{short circuit}} = 0$ since in this instance it is a voltage feedback circuit.

For the required values of E_o and Z_o, the open circuit loop gain $A\beta$ is determined.

The open loop gain A of the Charge Control Regulator is approximately -240 with a feedback factor β of 0.45, which gives an $A\beta$ of about -100.

The regulation factor is therefore

$$\frac{E_o}{E_n} = \frac{1}{1 + 100} \approx .01.$$

The output impedance with feedback was measured to be .01Ω. The charging voltage change due to input variations (24V-16V) is .08 volts and the change due to load variations (6A-1A) is .05 volts.

Total change is .13 volts or ± .065 volts. This corresponds to approximately ± .05% variation of charging voltage.

c. Ordinarily, the design of LC filters requires consideration of output ripple, transient response, and the critical inductance. The first two factors are relatively unimportant in battery charger design considerations. Consideration of the critical inductance, however, is of some value. When the Charge Control Regulator operates beyond the critical inductance region, it is liable to generate greater noise in the ground bus (since current flow is discontinuous) and result in adverse effects on the switching circuits, e.g. flip-flops, etc.

The equation for critical inductance (L_{CRIT}) is as follows:

$$L_{CRIT} = \frac{t_{off} \times R_L}{2}$$

Under worst case conditions, i.e. high line and light load, L_{CRIT} can be determined. The maximum input is assumed to be 24 volts, minimum load is 1 amp at 13 volts, $t_{off} = T(1-\frac{V_o}{V_{in}})$, $T = 200\mu S$, $t_{off} = 92\mu S$, thus

$$L_{CRIT} = \frac{92\mu S \times 13\Omega}{2}$$

$$= 600\mu h$$

B. AMPERE-HOUR METER (USED WITH AMPERE-HOUR METER TAPER CHARGE SYSTEM, SEE SCHEMATIC 59055.)

1. Operation

a. A block diagram of the Ampere-Hour Meter is shown in Figure 2-4. It consists of two basic subsystems. One is an Analog-to-Digital

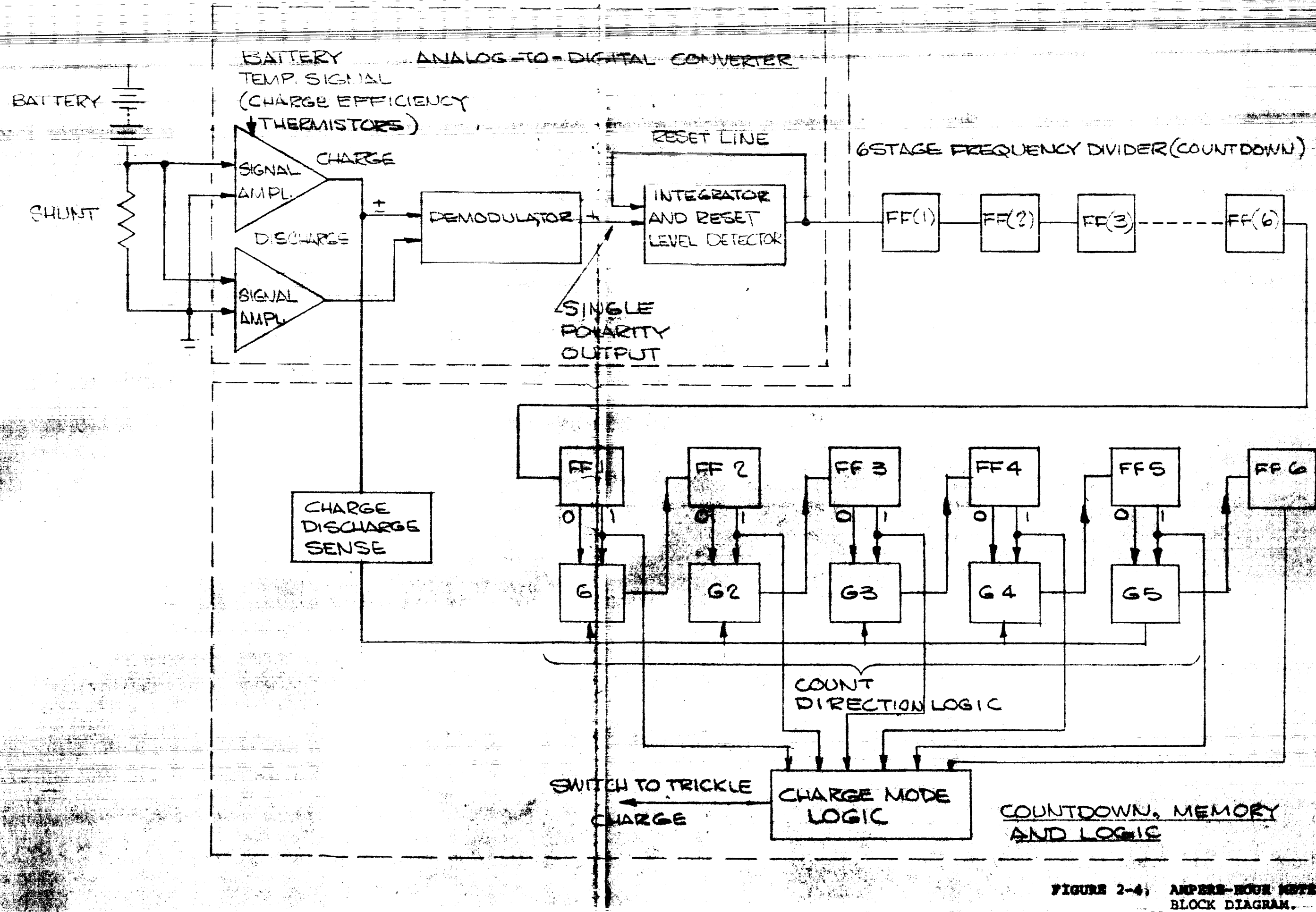


FIGURE 2-4, AMPERE-HOUR METER BLOCK DIAGRAM.

Converter where a voltage proportional to battery current is converted into a pulse rate. The second is the Countdown, Memory, and Logic system where the pulse rate is counted, stored, and converted into a switch-to-trickle-charge signal.

b. The Analog-to-Digital Converter consists of two DC Signal Amplifiers (charge and discharge), a Demodulator, and an Integrator and Reset Level Detector. The DC Signal Amplifiers provide a closed loop gain of 50 to step up the signal from the battery current shunt. This DC signal is bipolar and the polarity indicates charge or discharge. The Demodulator converts the bipolar signals into one of single polarity. This signal is used to control a constant current generator in a capacitor charging type Integrator. The Reset Level Detector provides a pulse output and resets the Integrator when the charging capacitor reaches a predetermined level. Thus, the Analog-to-Digital Converter generates a pulse train whose repetition rate is proportional to battery current.

c. The Countdown, Memory and Logic system counts and stores the pulses. Since the pulse rate is proportional to battery current, the total number in the Memory is the product of current and time, or amp-hours. The Memory is a six bit counter and has 64 distinct states. These 64 states are used to indicate total battery capacity. Therefore, each count for a 6 AH battery corresponds to approximately 0.1 ampere-hour added or removed. During the charge cycle, the Charge Mode Logic circuit detects when the Memory reaches the full charge state and generates the switch-to-trickle-charge signal.

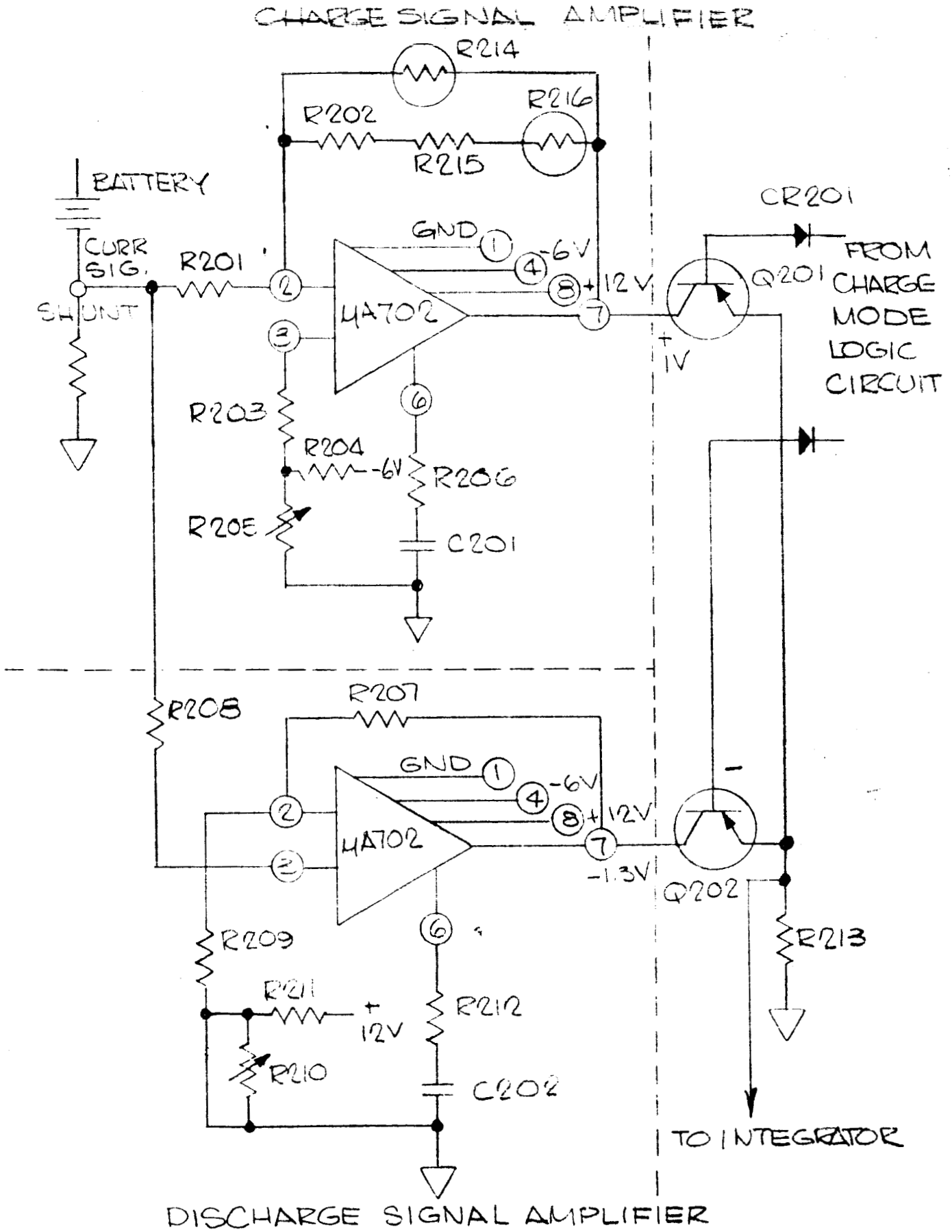


FIGURE 2-5. CHARGE AND DISCHARGE SIGNAL AMPLIFIERS.

d. The Charge Signal Amplifier and Discharge Signal Amplifier shown in Figure 2-5 consists of a Fairchild μA702 Integrated Differential Amplifier and operational type negative feedback. "Charge Efficiency Thermistors" form a part of the feedback resistor in the Charge Signal Amplifier. Their purpose is to correct the variations in recharge efficiency with temperature and are mounted directly on the battery. At room temperature the feedback resistor of the Charge Signal Amplifier is adjusted so that its gain is about 20% lower than that of the Discharge Signal Amplifier. When the Ampere-Hour Meter reads "fully charged" after the charging period, 20% more charge has been put into the battery than was removed during the discharge period.

e. Depending on the signals from the Charge Mode Logic circuit, Q201 and Q202 select and transmit to the Integrator either the output of the Charge Signal Amplifier or the output of the Discharge Signal Amplifier. During the discharge period, CR202 and Q202 conduct while CR201 and Q201 are cut off, thus connecting the output of the Discharge Signal Amplifier to resistor R213, which in turn feeds into the Integrator. During the charge period, CR201 and Q201 conduct while CR202 and Q202 are cut off.

f. Figure 2-6 shows the Integrator and Reset Level Detector. The Integrator is basically a Miller circuit. Unijunction transistor Q207 acts as a level detector. Pulses from Q207 are fed into Texas Instruments gate SN513A which serves as a pulse amplifier (PA1). The output pulse of

PA1 triggers the first flip-flop of the Frequency Divider (Countdown).

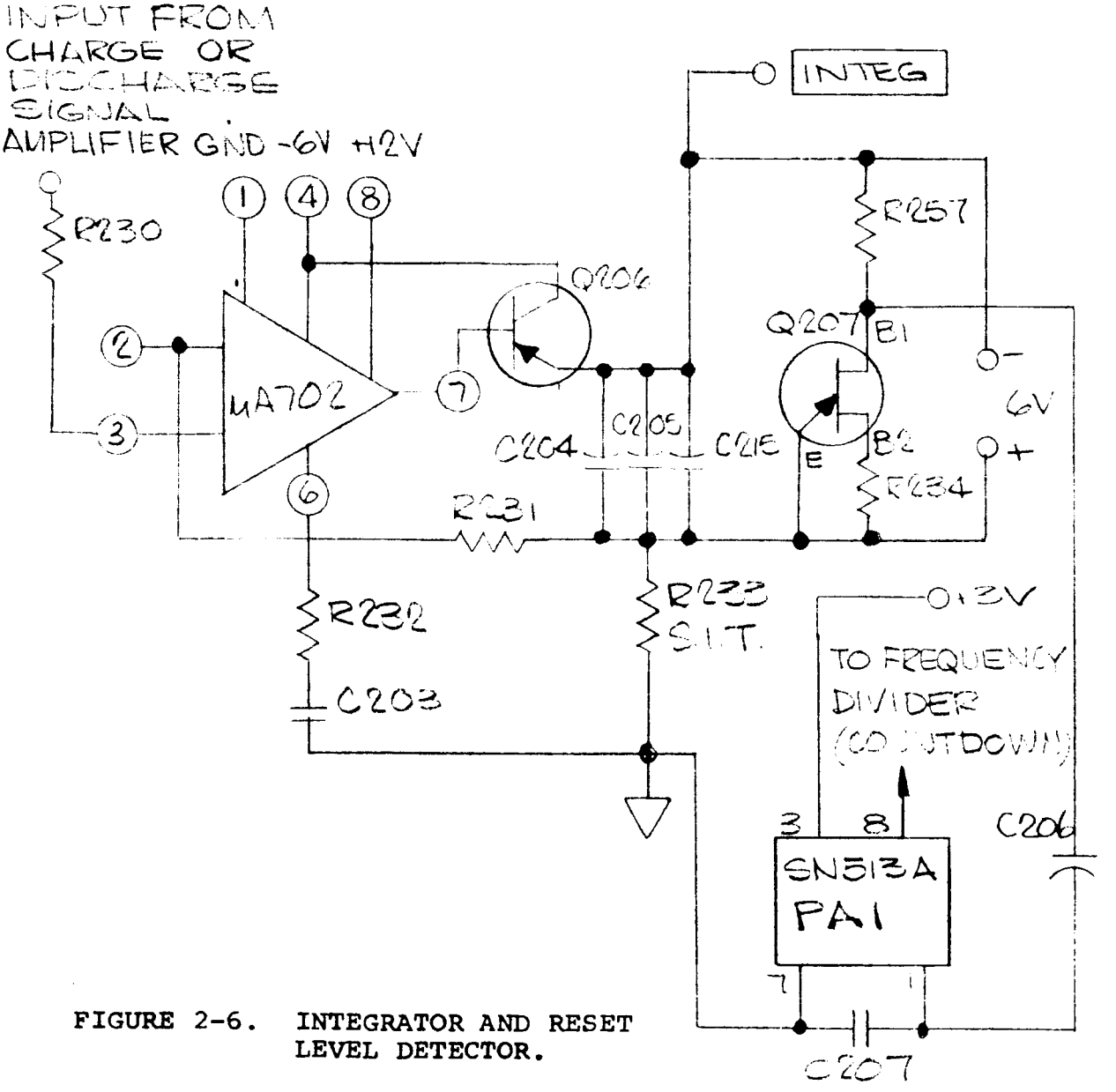


FIGURE 2-6. INTEGRATOR AND RESET LEVEL DETECTOR.

g. The Frequency Divider (Countdown) shown in Figure 2-7 consists of six flip-flops cascaded in series. Sixty-four pulses at the input correspond to one pulse at the output. The output pulse feeds into the Memory.

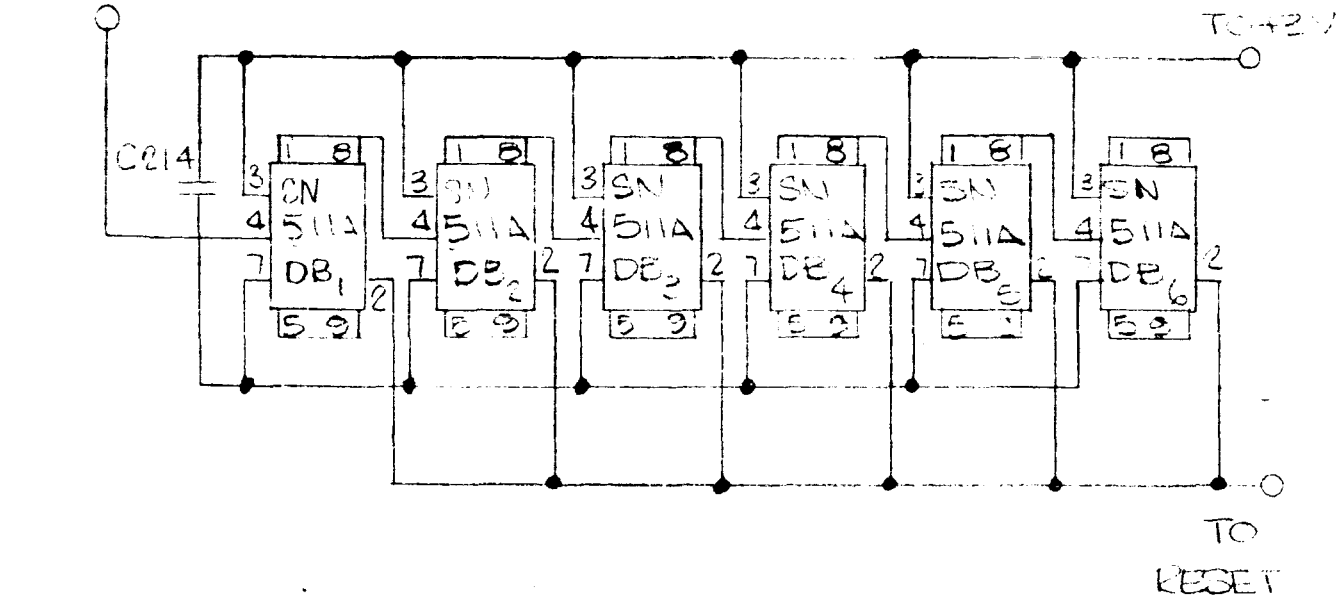


FIGURE 2-7. FREQUENCY DIVIDER (COUNTDOWN).

h. The Memory shown in Figure 2-8 is made up of Texas Instruments flip-flops SN511A and pulse "exclusive or" gates SN5191. If the Memory was used solely for the purpose of counting up or counting down, the "exclusive or" gates would not be needed. Depending upon the DC signal to the Memory from the Charge Mode Logic circuit, the gates function to make the Memory either count up or count down. The state of each flip-flop (B1 through B6) is defined to be "1" when pin 10 is high (positive 3V) and pin 6 is low (positive 5V). The flip-flop is triggered by the negative-

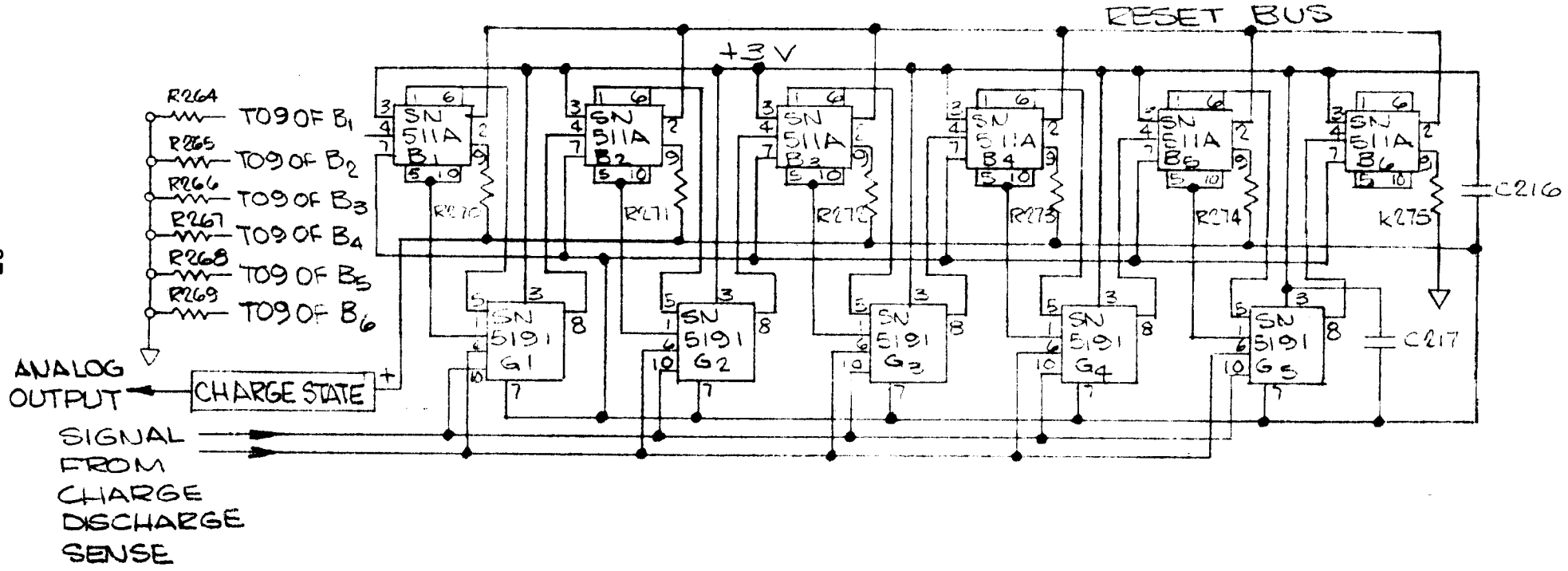


FIGURE 2-8. MEMORY.

going step. During the charge period, the "exclusive or" gate effectively connects pin 10 of flip-flop B1 to the flip-flop of the next higher significance, B2. Whenever B1 goes from "1" to "0", B2 is triggered, or the carry is forwarded. This is characteristic of the count-up function. In the discharge period, the "exclusive or" gate connects pin 5 of B1 to the input of B2, so that whenever B1 goes from "0" to "1", a carry is forwarded to B2. This is characteristic of the count-down function. Resistors R264 through R269 are connected to the outputs of the binaries and their values weighted in such a way that the terminal designated as "CHARGE STATE +" can be used to provide an analog output from the Memory. If the "CHARGE STATE +" terminal is connected to ground through a resistor, then the voltage across this resistor will be proportional to the number stored in the Memory.

2. <u>Design Parameters</u>

   a. The number of flip-flops in the Memory determines the accuracy of the Ampere-Hour Meter. Inherent indication error is $\frac{1}{2^n}$, where n is the number of flip-flops.

   b. The number of flip-flops in the Frequency Divider (Countdown) and the repetition rate is mainly governed by the choice of the Integrator capacitor C204, C205, and C215. A large capacitor cuts down the number of flip-flops by reducing the frequency. However, a large capacitor, especially one with stable temperature characteristics, is quite bulky. Optimum design should take into account the

space available for the capacitor, the accuracy required with variations of temperature, and the required pulse rate into the up-down counter (Memory). The integrator capacitor consists of three tantalum capacitors (C204,205,216) with a total capacitance of 167μf. (Wet tantalum capacitors were chosen since they have the lowest leakage current characteristics among tantalum capacitors.) The leakage current at 40°C is approximately 0.6μamps with a stress level of 3V. 500μamps through the capacitor corresponds to 5 amps current through the battery. At the battery current level of 1 ampere, the Integrator capacitor current is 100μamps, thus the error produced by the leakage current is about $\frac{1.8}{100}$, or 1.8%, and at 5 ampere battery current level, the leakage current is approximately $\frac{1.8}{500}$, or 0.4%. With this accuracy, one Integrator output pulse with a 3.5V sweep corresponds to 6 ampere-seconds (6 coulombs) of charge into the battery.

$$Q_{cap.} = I \times t = 600 \times 10^{-6} \times 1 \text{ second} = CV$$

$$\cong 167 \times 10^{-6} \text{uf} \times 3.5 \text{ volts}$$

The output pulse of the Frequency Divider (Count-down) with 6 flip-flops corresponds to

$$6 \text{ amp-sec} \times 2^6 \cong 0.1 \text{ Ampere-Hour.}$$

The six bit Memory section then, corresponds to $0.1 \times 2^6 = 6.4$ Ampere-Hours.

C. MAXIMUM POWER TRACKER (USED WITH ADHYDRODE-OPTIMUM TRACKING SYSTEM, SEE SCHEMATIC 57854.)

1. Operation

a. For the discussion which follows refer to Figure 1-2, Adhydrode-Optimum Tracking System Block Diagram, where the Maximum Power Tracker

is shown with relation to the system operation.

b. During the charging period, the duty cycle of the Pulse-Width Modulated Transistor Switch is adjusted by means of a feedback loop so that maximum power is delivered from the Solar Array to the Battery. The operation is analogous to adjusting the turns ratio of a transformer to match the load to an AC source impedance. In the circuit shown in Figure 2-9, if the turns ratio of the transformer is adjusted so that $R_S = n^2 R_L$, maximum power will be delivered from the AC source in the primary to the load R_L in the secondary. The analogous equation for the pulse-width modulated transistor switch is $\frac{V_o}{V_{in}} = \frac{t_{on}}{T}$: thus the effective turns ratio

$n = \frac{t_{on}}{T}$: hence, by varying t_{on} the "turns ratio" of the DC transformer (pulse-width modulated transistor switch) is changed.

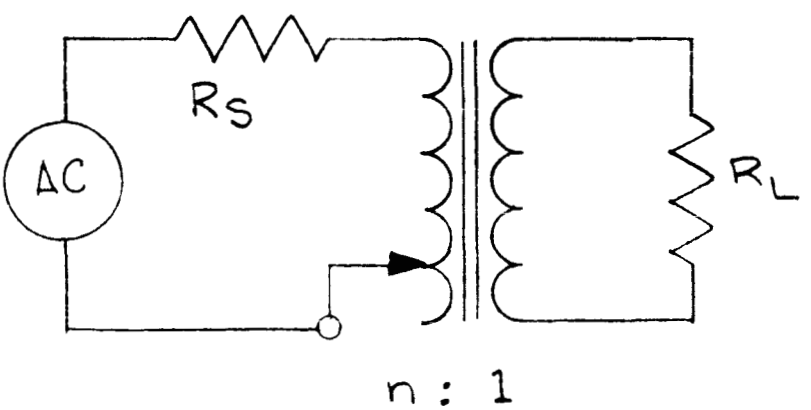


FIGURE 2-9. MAXIMUM POWER TRANSFERENCE UWING TRANSFORMER.

c. In the Maximum Power Tracker, maximum power transference from the Solar Array to the Battery is accomplished by changing the duty

cycle of the Transistor Switch, which changes the load line from A to B as shown in Figure 2-10.

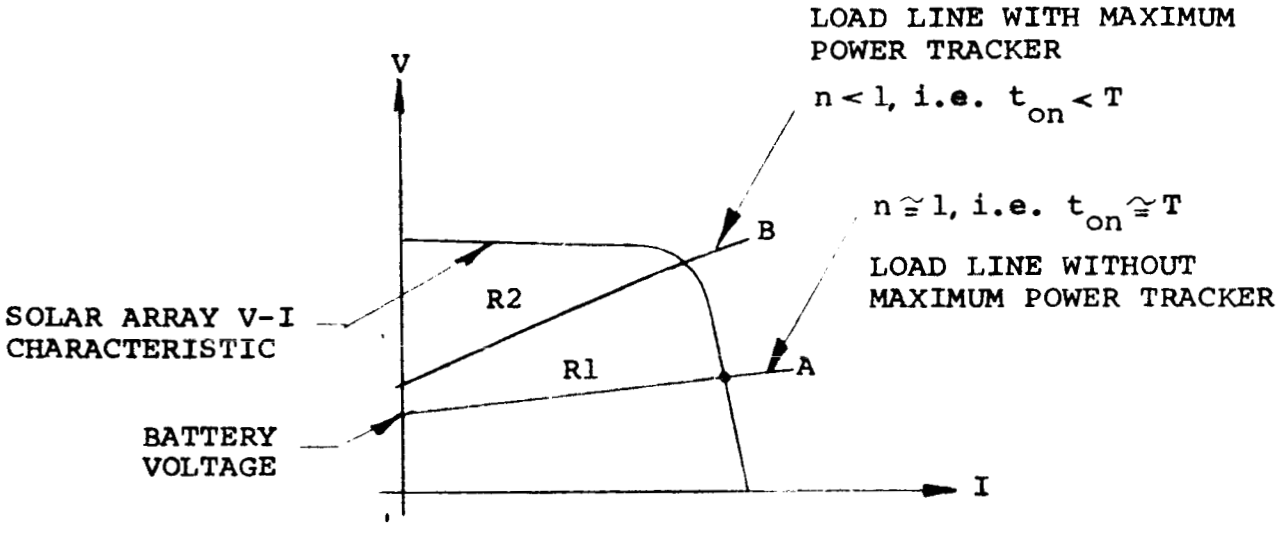


FIGURE 2-10. EFFECTS OF CHANGING THE DUTY CYCLE OF THE TRANSISTOR SWITCH.

d. When the feedback loop of the system is closed, the duty cycle of the Transistor Switch will adjust in such a manner as to intersect with the maximum power point shown on Figure 2-11.

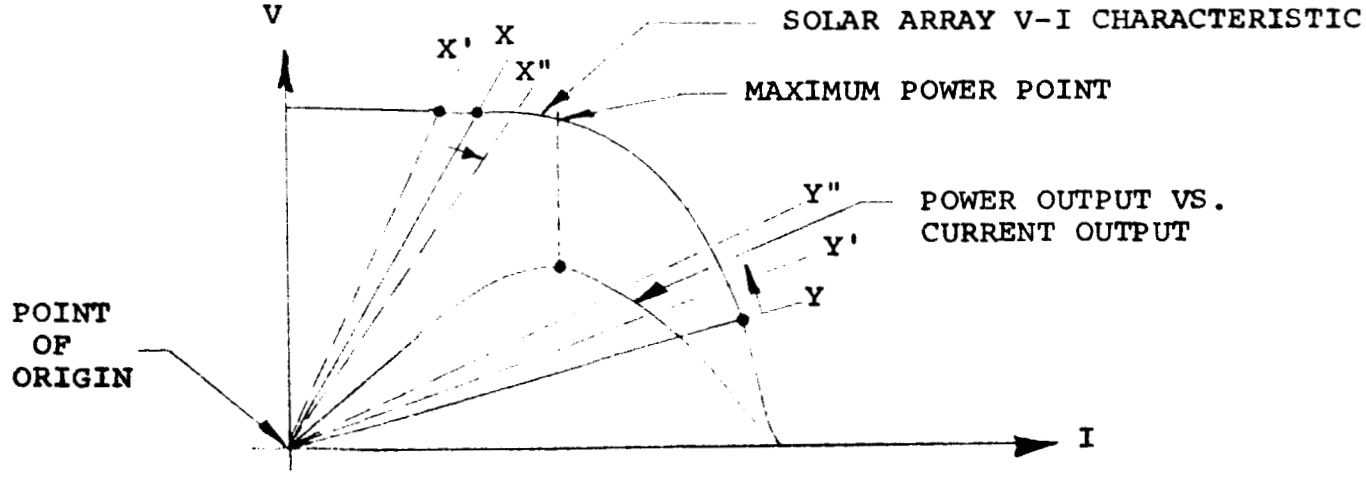


FIGURE 2-11. INTERSECTION OF TRANSISTOR SWITCH DUTY CYCLE WITH MAXIMUM POWER POINT.

In visualizing how this action is accomplished, consider a resistive load at the output instead of a resistance in series with an ideal battery (which is equivalent to the actual battery). Assume that the duty cycle of the Transistor Switch is such that the load line appears as X in Figure 2-11. The positive going Perturbing Signal decreases the duty cycle of the Transistor Switch by momentarily shifting the load line to X'. This action decreases the output power and causes a negative going sense signal to appear at the load. The negative going sense signal energizes Phase Detector A. Phase Detector A causes the Differential Amplifier output to swing in a direction which increases the duty cycle. This increase shifts the load line to X", or toward the maximum power point. If, on the other hand, the duty cycle of the Transistor Switch is such that the load line appears as Y in Figure 2-11, the positive going perturbing signal decreases the duty cycle of the Transistor Switch as before, but output power will increase because the load line now shifts to Y'. As a result of this action, a positive going sense signal appears at the load. The positive going sense signal energizes Phase Detector B. Phase Detector B causes the Differential Amplifier output to swing in a direction which decreases the duty cycle. This will shift the load line to Y", or toward the maximum power point. In the case of a battery load, the load line will not pass the point of origin, as is the

case with a resistive load, and the slope of the load line will be much smaller.

e. The Pulse-Width Modulated Transistor Switch as shown in Figure 2-12 is essentially a power transistor chopper (Q4) with an LC Filter at the output. Three signals are superimposed on the base of Q9: a high frequency (10 KC) synchronizing signal from the Auxiliary Power Supplies, a DC signal from the Differential Amplifier, and a low frequency square wave (10 CPS) from the Perturbing Signal Source. Q9 will be turned on and off by the synchronous signal. However, the duty cycle of the switching transistor Q8 depends on the level of the slowly varying signals (the DC signal plus the 10 CPS perturbing signal) supplied to Q9. Q8 is connected in such a way that whenever Q9 is "on", Q8 is "off" and vice versa. Switching transistor Q8 drives Q6, which in turn drives the Darlington connected transistors Q4 and Q5. Thus the duty cycle of the switching power transistor Q4 is controlled by the DC signal level into Q9. The "end of change" signal is applied to the base of Q7 and turns off Q4.

f. The Inverting and Non-Inverting Amplifiers are operational type feedback amplifiers using Fairchild μA702C Integrated Differential Amplifiers. They are shown in Figures 2-13 and 2-14.

g. The output of the Phase Detector, shown in Figure 2-15, may appear as waveform "a", "b", or "c". Waveform "a" represents the condition when the input signal from the Inverting or Non-Inverting Amplifier, and the reference signal from the Perturbing Signal Source are completely in-phase and maximum output to the Differential Amplifier is the result.

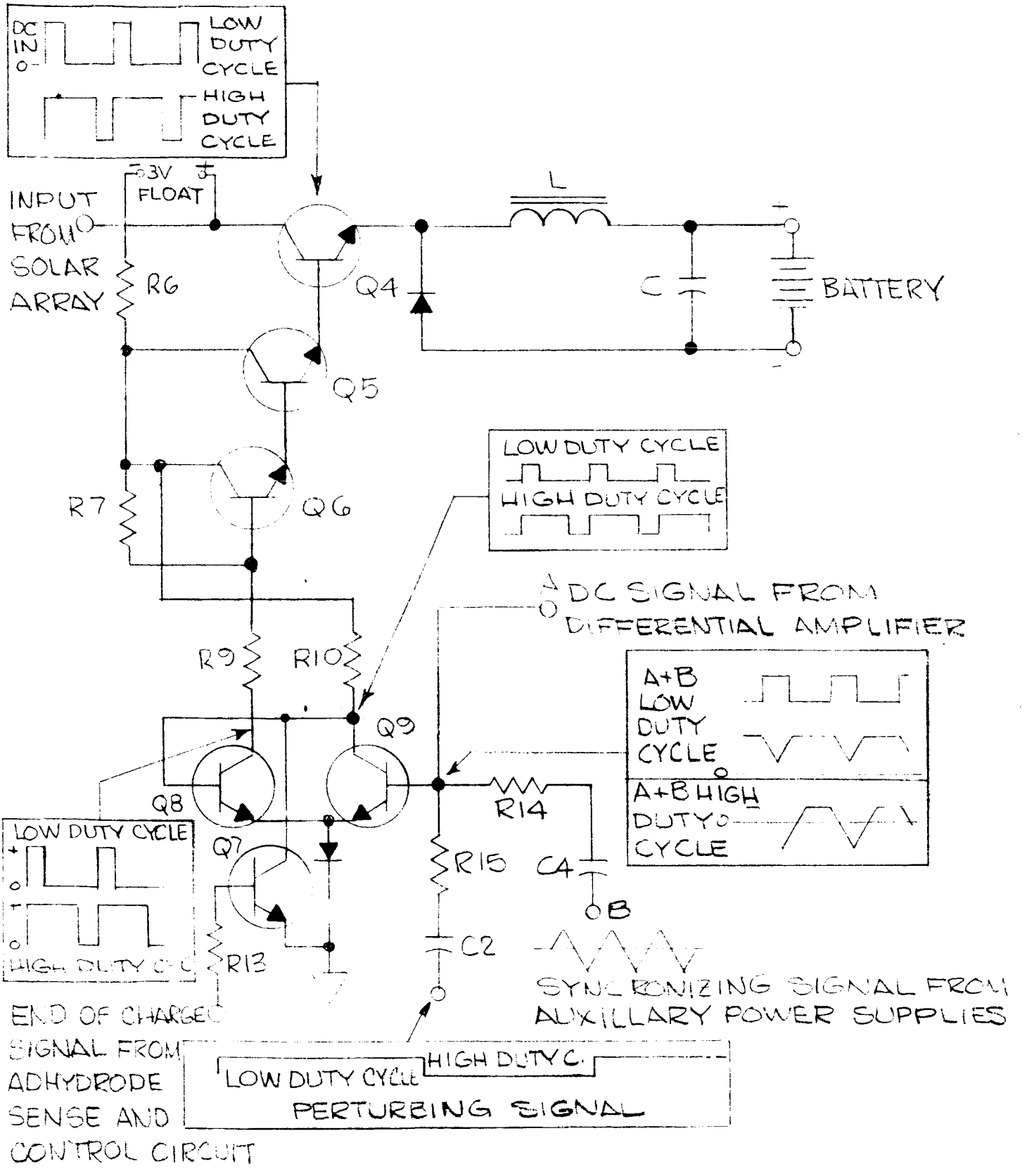


FIGURE 2-12 PULSE-WIDTH MODULATED TRANSISTOR SWITCH, SIMPLIFIED DIAGRAM

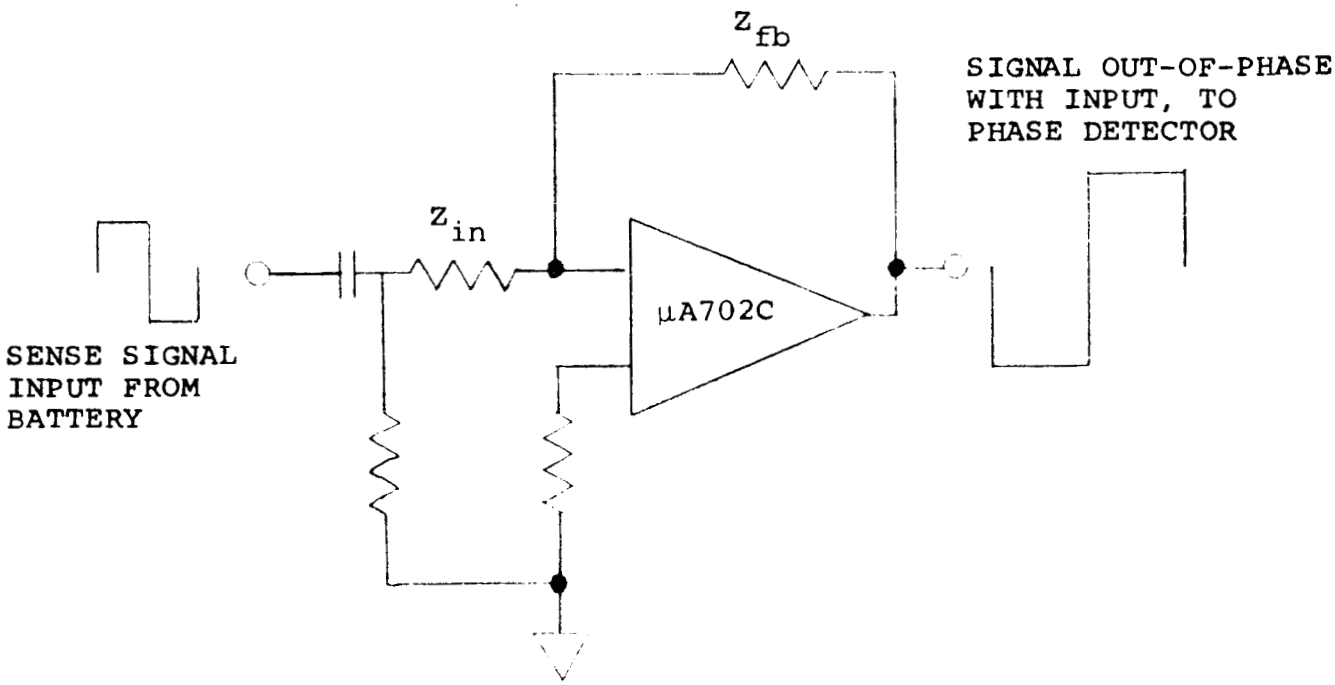


FIGURE 2-13. INVERTING AMPLIFIER SIMPLIFIED DIAGRAM.

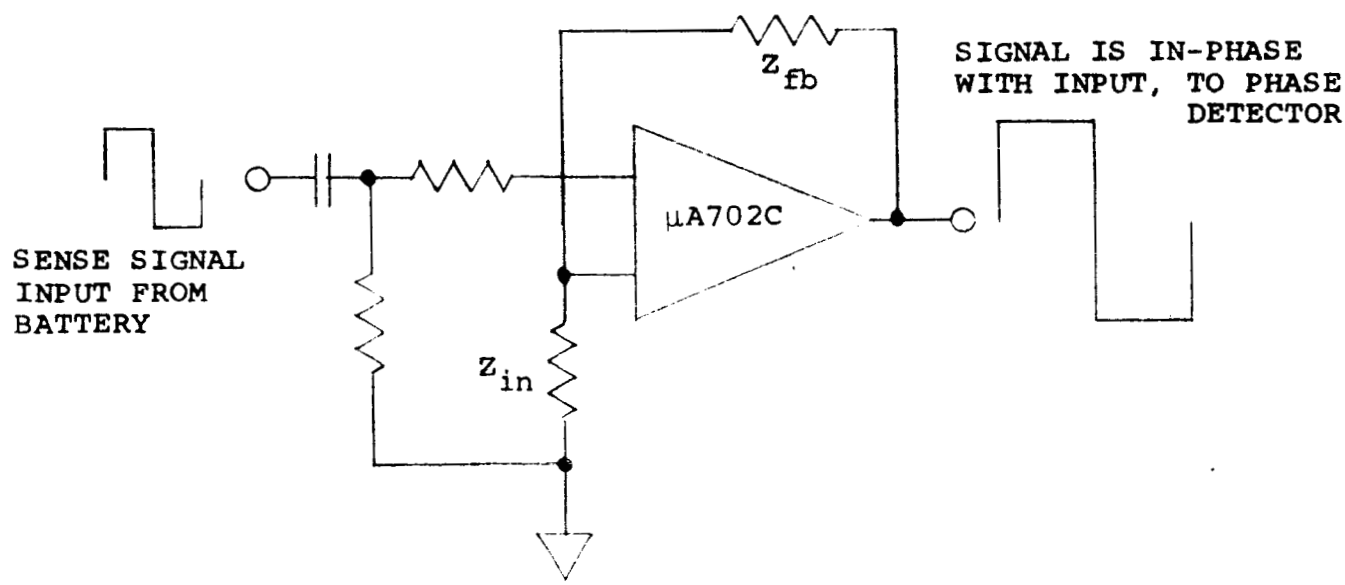


FIGURE 2-14. NON-INVERTING AMPLIFIER SIMPLIFIED DIAGRAM.

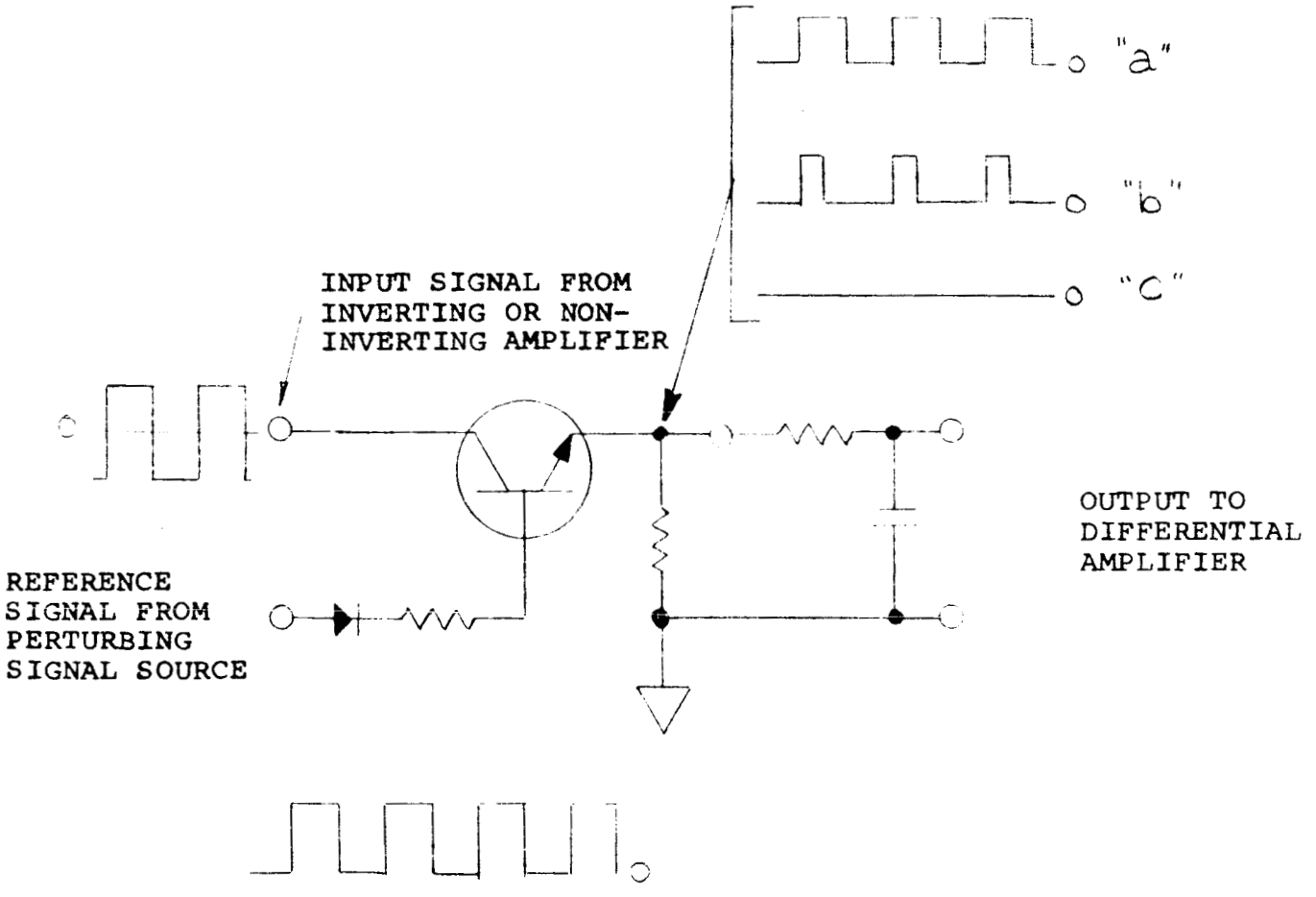


FIGURE 2-15. PHASE DETECTOR A OR B AND OUTPUT WAVEFORMS.

Waveform "c" represents the condition when the input signal is completely out-of-phase with the reference signal and the output is then zero. The waveform of "b" will result when the input signal is partially in-phase (or out-of-phase) with the reference signal. The output is then non-zero, but less than that of condition "a". The waveforms described above actually apply to the period when the Maximum Power Tracker is "hunting" the maximum

power point. While operating at the maximum power point the waveforms will be as in Figure 2-16. In this instance, the input and both Phase Detector outputs are ideally zero. Actually the input contains some noise voltages of low amplitude.

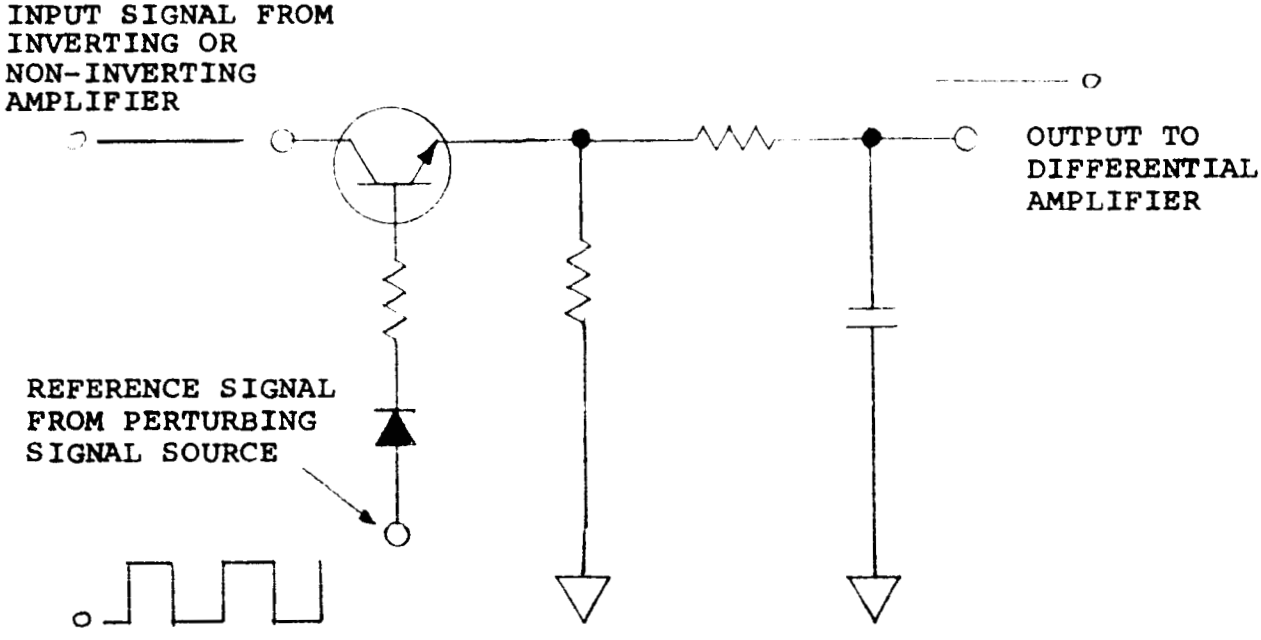


FIGURE 2-16. PHASE DETECTOR OUTPUT WAVEFORM AT MAXIMUM POWER POINT OPERATION.

h. The Differential Amplifier shown in Figure 2-17 is a Fairchild μA702C, used without local feedback. An RC compensation network at the output is used to filter out the 10 CPS component. The DC output signal controls the Pulse-Width Modulated Transistor Switch described previously.

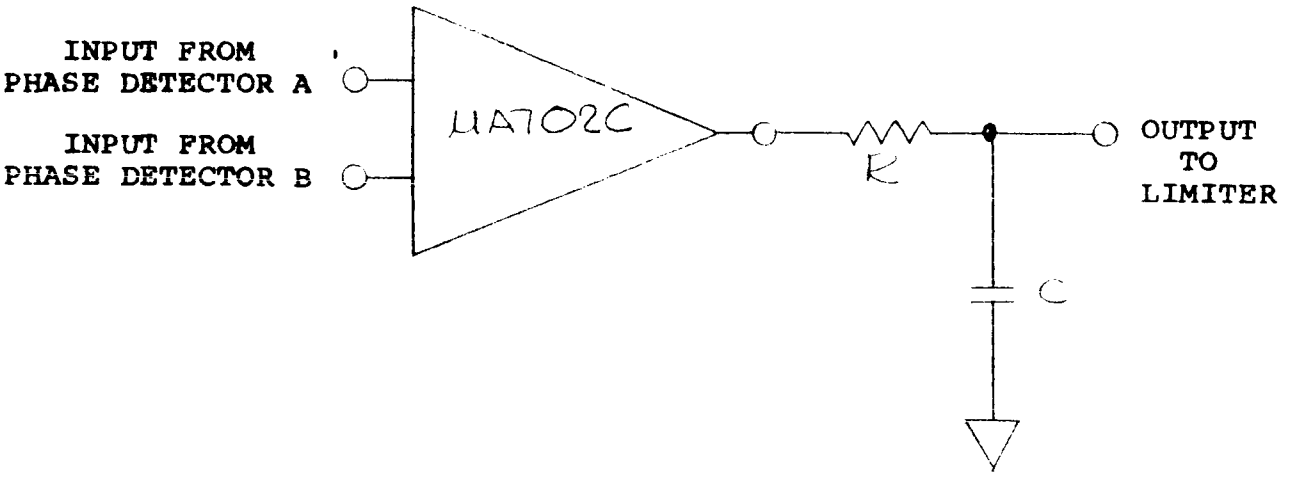


FIGURE 2-17. DIFFERENTIAL AMPLIFIER.

i. The function of the Limiter is to limit the excursion of the DC signal feeding into the Transistor Switch. Without the Limiter, it is possible for the DC signal to swing far enough during the "hunting" period to cut off or saturate the Transistor Switch. If this happens, the perturbing signal will be ineffective. Perturbation of the duty cycle of the Transistor Switch will not occur and there would be no low frequency ripple at the battery, which is essential to the Maximum Power Tracker operation. Thus, the Transistor Switch could latch in a cut-off or saturated condition. The Perturbing Signal Source (10 CPS oscillator) supplies the perturbing signal to the Pulse-Width Modulated Transistor Switch, and the

reference signal to Phase Detector A and B. It is basically an astable multivibrator with a buffer. This is shown in Figure 2-18.

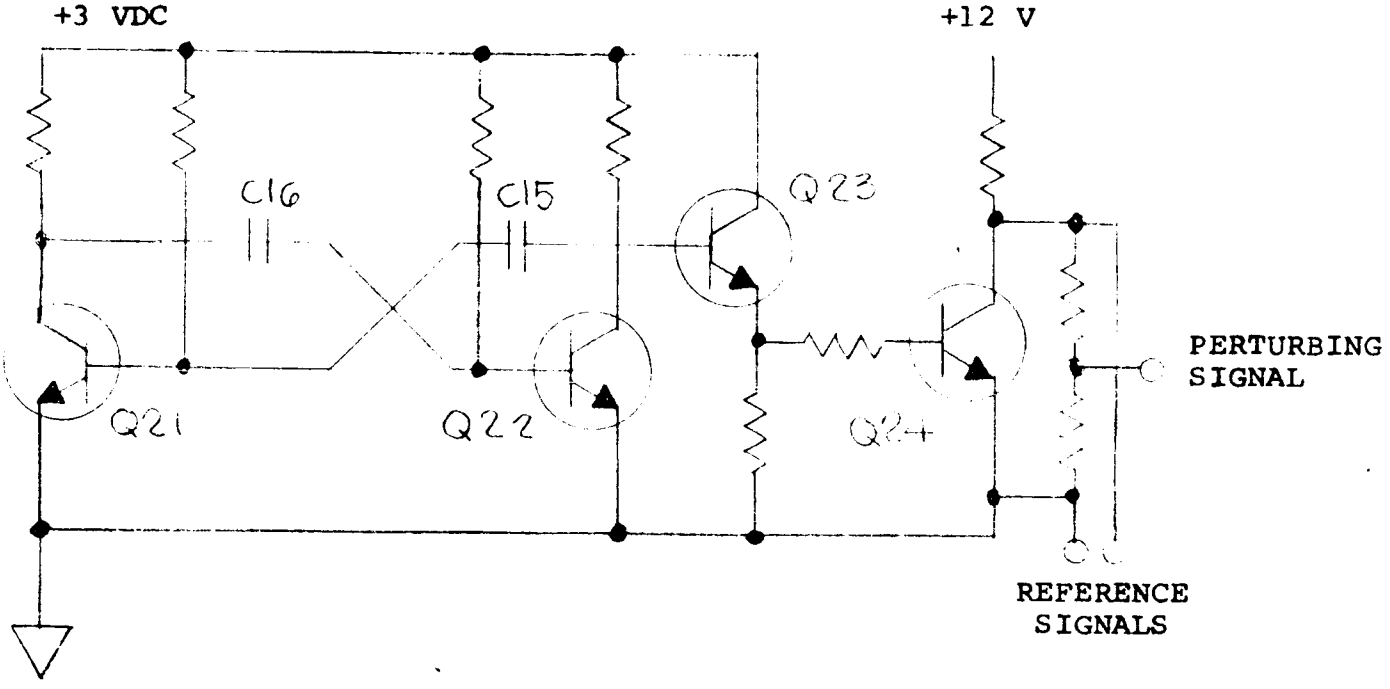


FIGURE 2-18. PERTURBING SIGNAL SOURCE.

j. The Trickle Charge Circuit, shown in Figure 2-19, is turned on by a positive voltage at the base of Q3. When Q3 turns on, Q2 also turns on and provides a path from the current source consisting of Q1, associated resistors, and the voltage source to the battery. The "end of charge" signal driving Q3 is also applied to the base of transistor Q7 (Figure 2-12) of the Pulse-Width Modulated Transistor Switch, and turns off Q4.

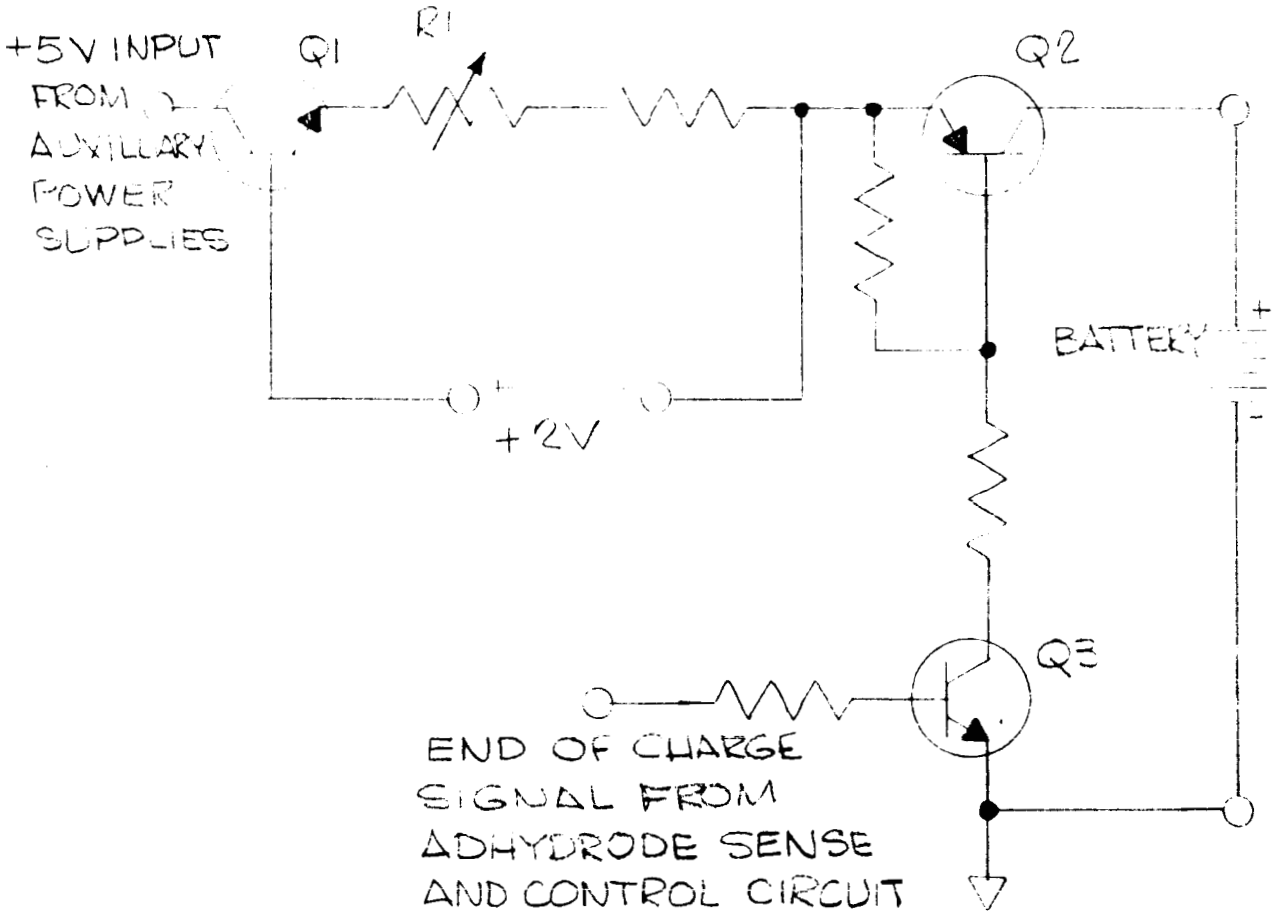


FIGURE 2-19. TRICKLE CHARGE CIRCUIT SIMPLIFIED DIAGRAM.

2. Input-Output Equations

a. Figure 2-20A shows the characteristics of a Solar Array. Load line "A" represents the condition when the battery is directly connected to the Solar Array during the charge period. Although there is a non-dissipative power transfer, it is not an optimum match. This results in the operating point at "x", which corresponds to point "a" in Figure 2-20B, and shows much less power output than P_{max}.

b. Load line "B" represents the condition when the Maximum Power Tracker is in control, and results in the operating point at "y", which corresponds to the maximum Solar Array output. The Maximum Power Tracker has effectively changed the load line "A" to load line "B" to obtain maximum power.

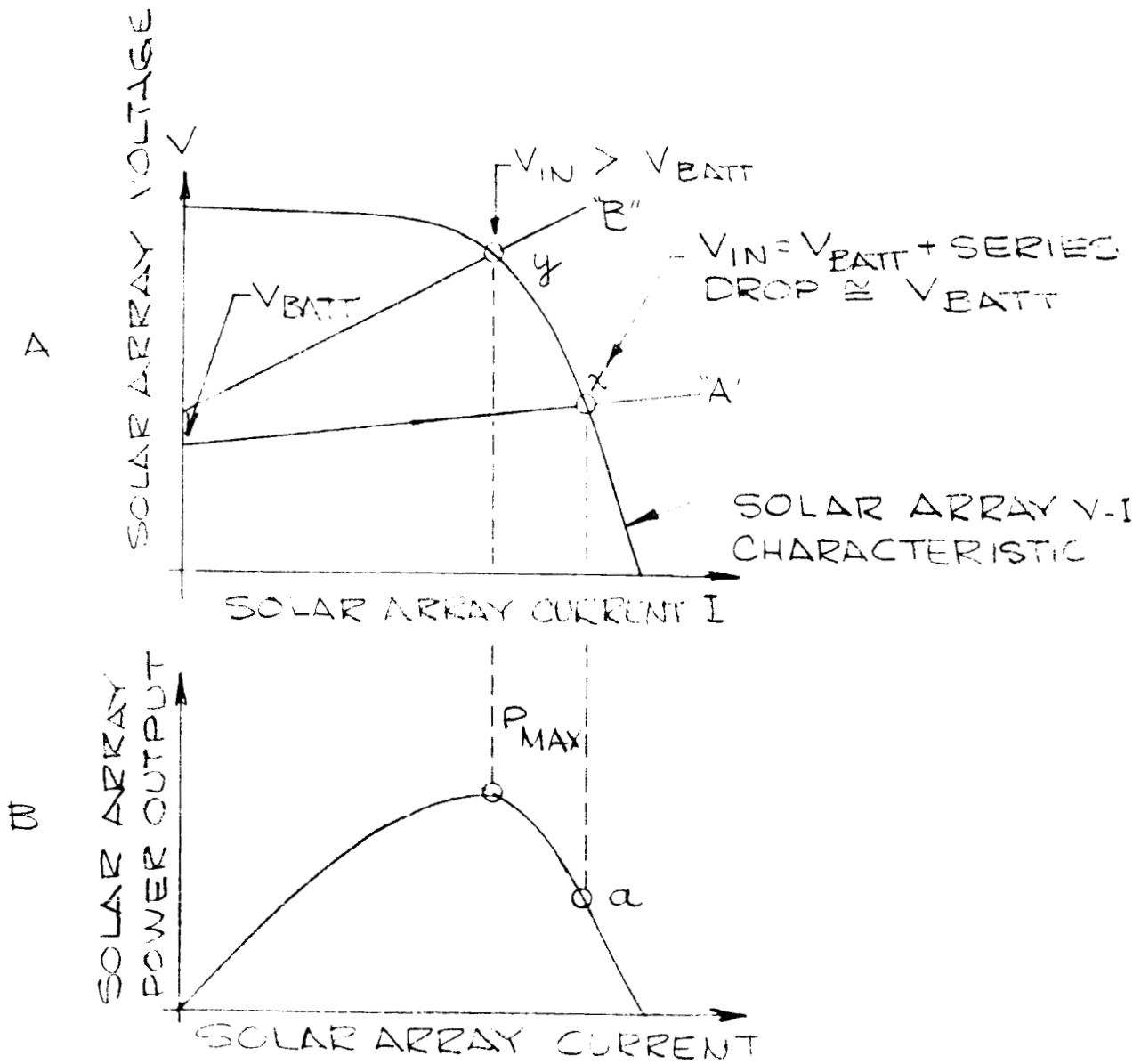


FIGURE 2-20. SOLAR ARRAY CHARACTERISTICS.

c. The shifting of the load line can be effected through impedance changes.

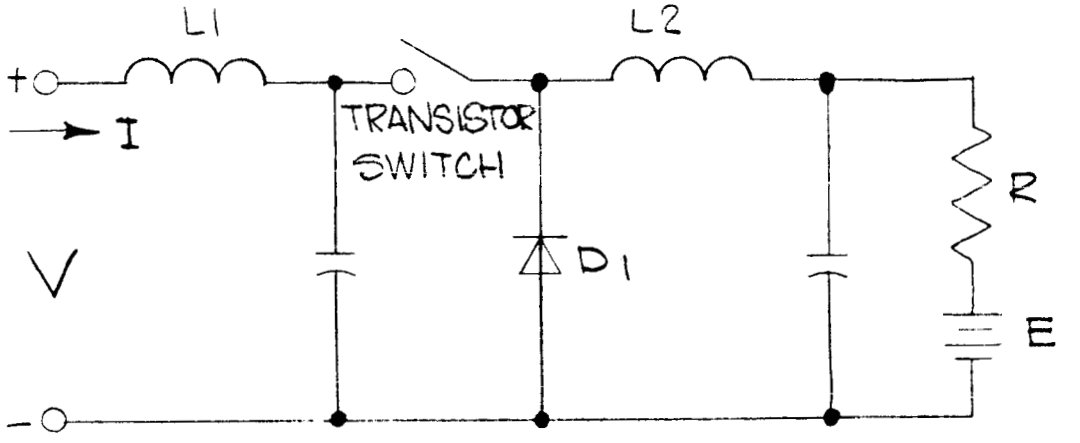


FIGURE 2-21. TRANSISTOR SWITCH FUNCTION, SIMPLIFIED DIAGRAM.

In Figure 2-21, R, in series with the ideal battery E, represents the actual battery at a certain moment. The V-I characteristic is load line "A" in Figure 2-20A with proper polarity. L1 and L2 are large enough so that current through them is essentially DC. Wire resistance in L1 and L2 is negligible. Assume that the transistor switch and diode D1 have no losses. When the transistor switch is closed during the entire chopping period, the V-I characteristic of the input is simply that of a battery, R in series with E. If the transistor switch now closes and opens with a certain duty cycle, at an input frequency of 5 KC, the V-I characteristic will change. If the input

current is I, then the current into the load (battery in this case) is $\frac{I}{n}$. Power delivered to the ideal battery is $P_E = \frac{I}{n} E$, and by resistance $P_R = \left(\frac{I}{n}\right)^2 R$. Total power delivered to the battery is then $P_T = P_E + P_R = \frac{I}{n} E + \left(\frac{I}{n}\right)^2 R$. This is also the power (V X I) drawn at the input, since all components between the input and the load were assumed to be non-dissipative.

$$P_T + V_I = \frac{I}{n} E + \left(\frac{I}{n}\right)^2 R$$

$$\text{Therefore, } V = \frac{E}{n} + \frac{I}{n^2} R \qquad (1)$$

Equation (1) is in the form of $V = V_o + R_o I$, which is the characteristic of a battery with an open circuit voltage of V_o, and internal resistance of R_o. Thus, for the input, the battery characteristic has changed from one with an open circuit voltage of E and internal resistance of R to that of $\frac{E}{n}$ and $\frac{R}{n^2}$.

d. The basis of the Maximum Power Tracker is adjusting the duty cycle of the Transistor Switch to the point where the intersection of the Solar Array characteristic and the load line, effectively modified by the Maximum Power Tracker, is at point "y" of Figure 2-20A.

3. Design Parameters

a. Designing the Pulse-Width Modulated Transistor Switch consisted mainly of choosing the proper

transistors and heat sinks for efficient handling of the required power. Considerations of turn-on and turn-off time of the switching transistors were important. The approximate equation for the collector power dissipation in a switching transistor may be determined by assuming the current and voltage waveforms are as shown in Figure 2-22.

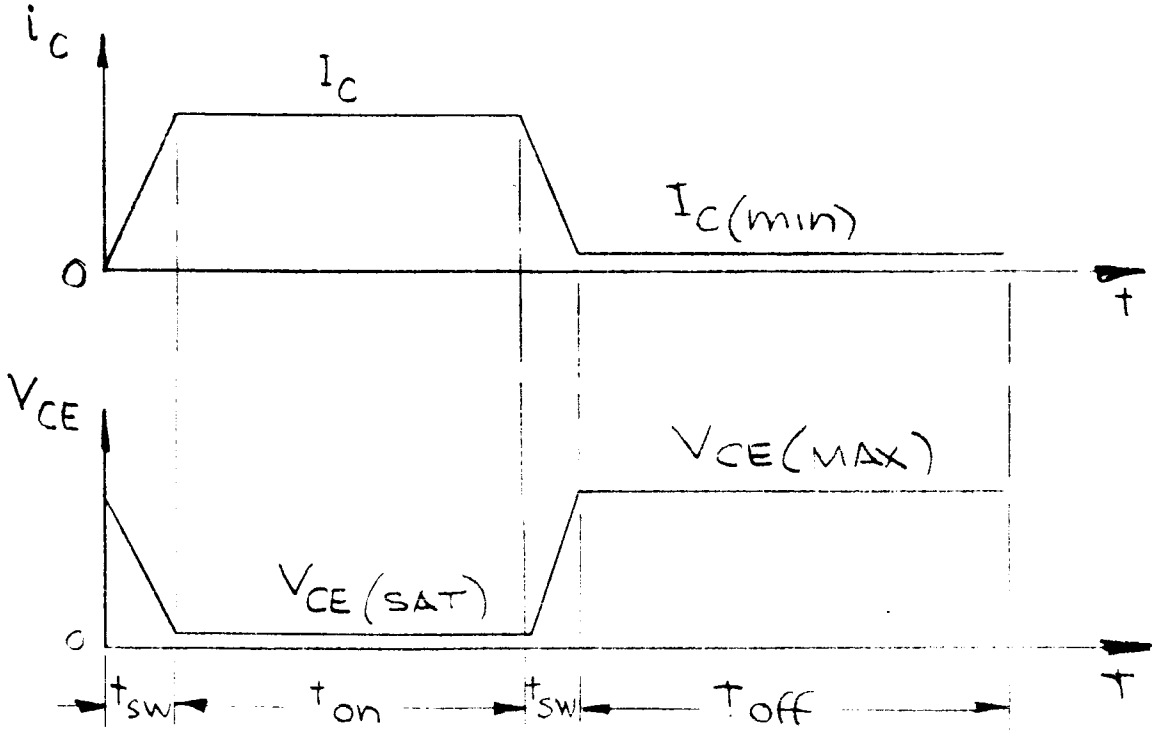


FIGURE 2-22. IDEALIZED SWITCHING WAVEFORMS.

When the transistor is "off" the power dissipation is

$$P_{C1} = \frac{t_{off}}{T} V_{CE(max)} I_{C(min)}, \quad (1)$$

where T = period of the waveform.

During the "on" time

$$P_{C2} = \frac{t_{on}}{T} V_{CE(sat)} I_C. \quad (2)$$

Neglecting $I_{C(min)}$ during the switching interval, the collector current and collector-to-emitter voltage may be written as follows:

$$i_c = I_C \frac{t}{t_{sw}}, \quad (3)$$

and $$V_{CE} = V_{CE(max)} - \left[V_{CE(max)} - V_{CE(sat)}\right] \frac{t}{t_{sw}}. \quad (4)$$

The energy dissipated during one switching interval is

$$E_{C3} = \int_0^{t_{sw}} i_c V_{CE} \, dt. \quad (5)$$

After integration and grouping of terms equation (5) becomes

$$E_{C3} = \frac{t_{sw} I_C}{6} \left[V_{CE(max)} + 2 V_{CE(sat)}\right] \quad (6)$$

Thus, the total collector power dissipation is

$$P_C = \frac{t_{off}}{T} V_{CE(max)} I_{C(min)} + \frac{t_{on}}{T} V_{CE(sat)} I_C + \frac{t_{sw}}{T} \frac{I_C}{3} \left[V_{CE(max)} + 2 V_{CE(sat)}\right]$$

$$P_C = \frac{1}{T} \left[t_{off} V_{CE(max)} I_{C(min)} + t_{on} V_{CE(sat)} I_C + t_{sw} I_C/3 \left(V_{CE(max)} + 2V_{CE(sat)}\right)\right]$$

Since the power loss is directly proportional to the chopping frequency, operation at the lowest possible frequency is desired. However, an increase in size of the filter choke and other magnetic components in the system limits the minimum frequency. The Pulse-Width Modulated Transistor Switch is operated at a frequency of 5 KC, under which condition the average efficiency of the transistor switch is 92% and the magnetic components will be of reasonable size.

b. The gain of the Inverting and Non-Inverting Amplifiers had to be large enough so that the output swings were sufficient to energize the Differential Amplifier at the worst signal condition. The worst signal condition occurs when the Solar Array voltage is at minimum, i.e., 16 volts. Assuming the current limit of the Solar Array is at 7 amps,

$$\Delta p = 7 \times 16(n + \Delta n) - 7 \times 16 \times n = 112(\Delta n)$$

where Δp: change of power delivered to the battery

n: duty cycle of the Transistor Switch

Δn: change of the duty cycle due to the perturbing signal, typically $\pm 5\%$

$$\Delta p = (112)(.05) = 5.6 \text{ watts.}$$

Change of battery current

$$\Delta I = \frac{5.6 \text{ watts}}{14.6 \text{ volts}} \simeq .4 \text{ amps.}$$

Voltage change of the battery due to the perturbing signal is, then,

ΔV = .4 amps X Internal Resistance of Battery ($\simeq .03\Omega$)

$$\Delta V = .01 \text{ volt.}$$

Gain of the Inverting and Non-Inverting Amplifiers is

$$\frac{A}{1-A\beta}$$

where A: Open-loop gain of μA702C (typically -2600)

$$\beta \text{ (feedback ratio)} = \frac{1K}{422K} = \frac{1}{422}$$

$$A_{fb} = \frac{2600}{1 + \frac{(2600)}{422}} = \frac{2600}{1 + 6.15} = 363$$

A_{fb} = closed-loop gain of amplifier

Input to the Phase Detector

= .01V X 363 = 3.6 volts.

This is the approximate magnitude of the square wave input to the Phase Detector A or B. This results in a settling time of 10 seconds in the Maximum Power Tracker.

c. It was found experimentally that the system as designed failed to function with the perturbing signal frequency above 25 cycles per second. Time was not adequate to investigate the limiting frequency.

d. An RC lag network at the output of the Differential Amplifier stage eliminated the oscillation of the system. For a given time constant, RC, increase of R permitted the use of a small capacitor at the expense, however, of decreasing the loop gain; whereas, a small R and a large C increased the bulk. A compromise was made between size and accuracy. The RC product of about 7 seconds was found to be a suitable value which eliminated the oscillation of the system and yielded about 10 seconds response time. Accuracy of the system varied approximately as shown in Figure 2-23.

As the capacitance increased and resistance decreased, 660μf capacitance was chosen for the breadboard since increasing the capacitance over this point did not change the accuracy significantly.

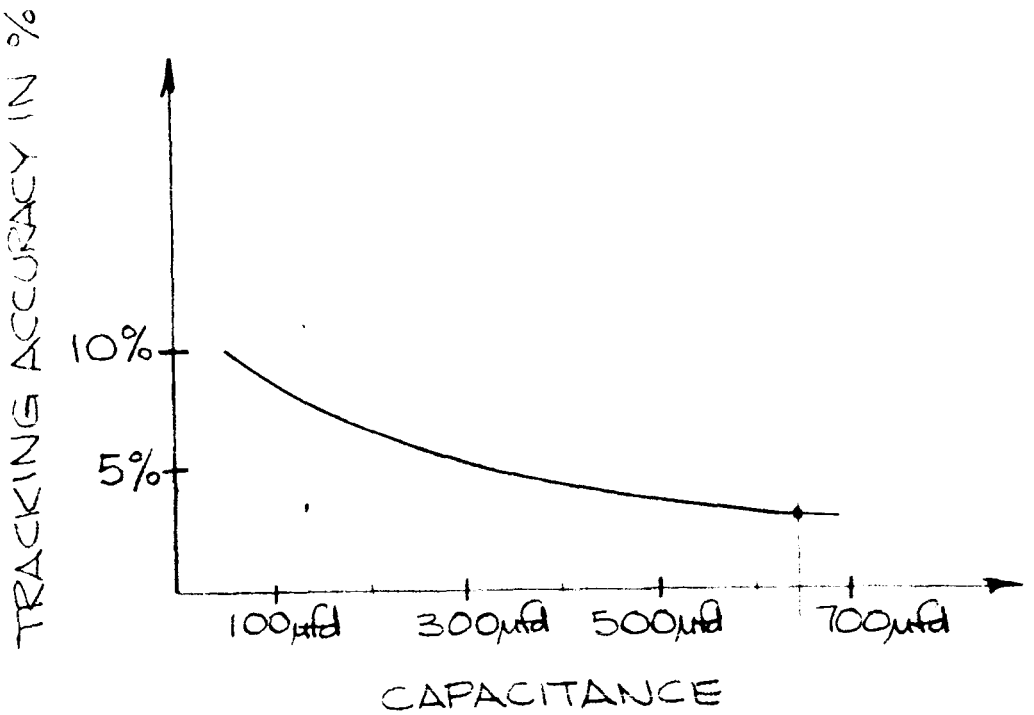


FIGURE 2-23. CAPACITANCE VS TRACKING ACCURACY.

D. ADHYDRODE SENSE AND CONTROL CIRCUITS (PART OF BATTERY CHARGER CONTROL SYSTEM USING MAXIMUM POWER TRACKER, SEE SCHEMATIC 57854.)

1. Operation

a. The Adhydrode Sense and Control Circuit consists of the Magnetic Amplifier, Filter, and a Pulse Amplifier (see Figure 2-24). When the sum of the battery adhydrode voltages

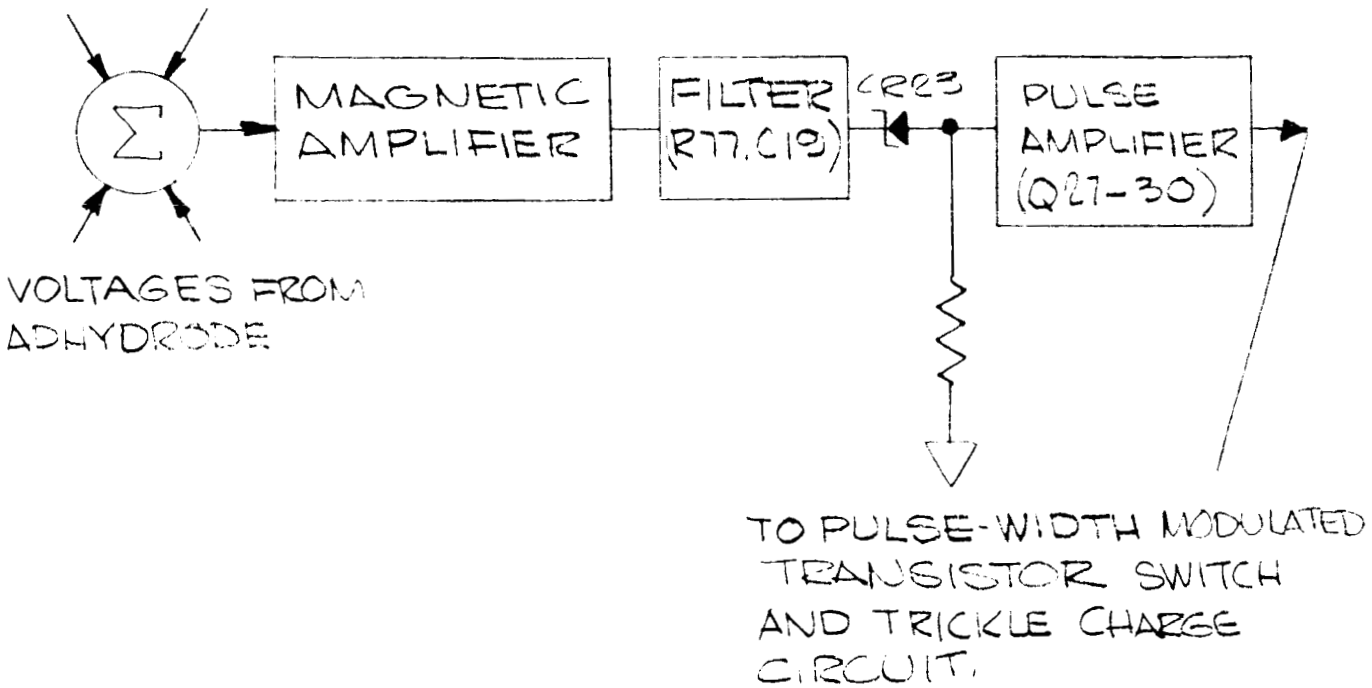


FIGURE 2-24. ADHYDRODE SENSE AND CONTROL CIRCUIT BLOCK DIAGRAM.

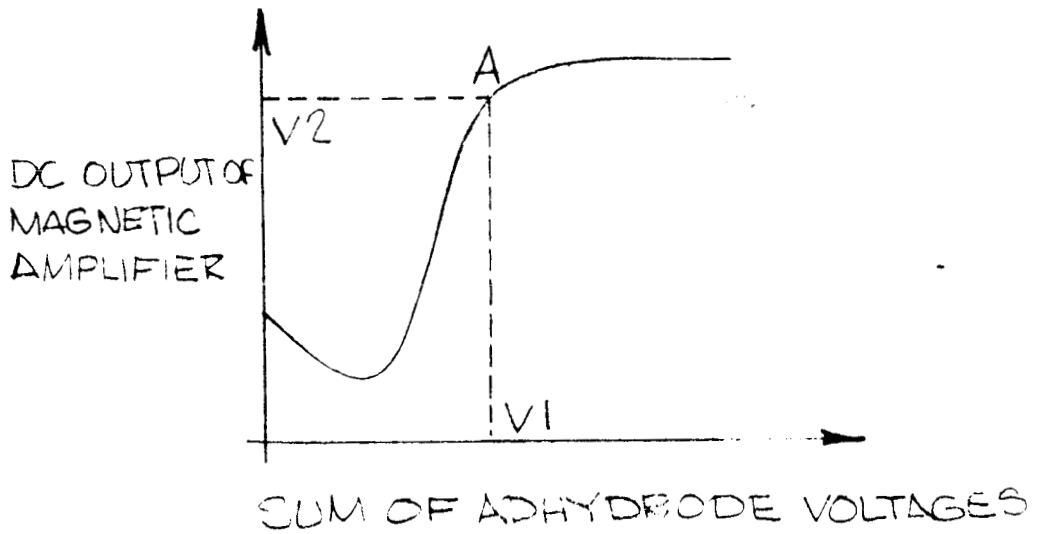


FIGURE 2-25. MAGNETIC AMPLIFIER CHARACTERISTICS.

reaches the value of V1, as shown in Figure 2-25, the output of the Magnetic Amplifier is V2, which is the threshold value of the zener diode (CR23) breakdown voltage. When the zener diode breaks down, the Pulse Amplifier (Q27-Q30) generates a signal which is used to turn off the Pulse-Width Modulated Transistor Switch and energize the Trickle Charge Circuit.

b. The Magnetic Amplifier shown in Figure 2-26 is a self-saturating type doubler circuit. Bias current is supplied from a current source (Q31). The control winding shown may be any number of windings to sense the adhydrode voltage from the battery cells, in this case four windings (pins 1 through 8). Total control current is then the algebraic sum of currents in all the windings. Current flowing in each winding is the adhydrode voltage divided by the sum of the winding resistance and any resistance which is in series with the winding.

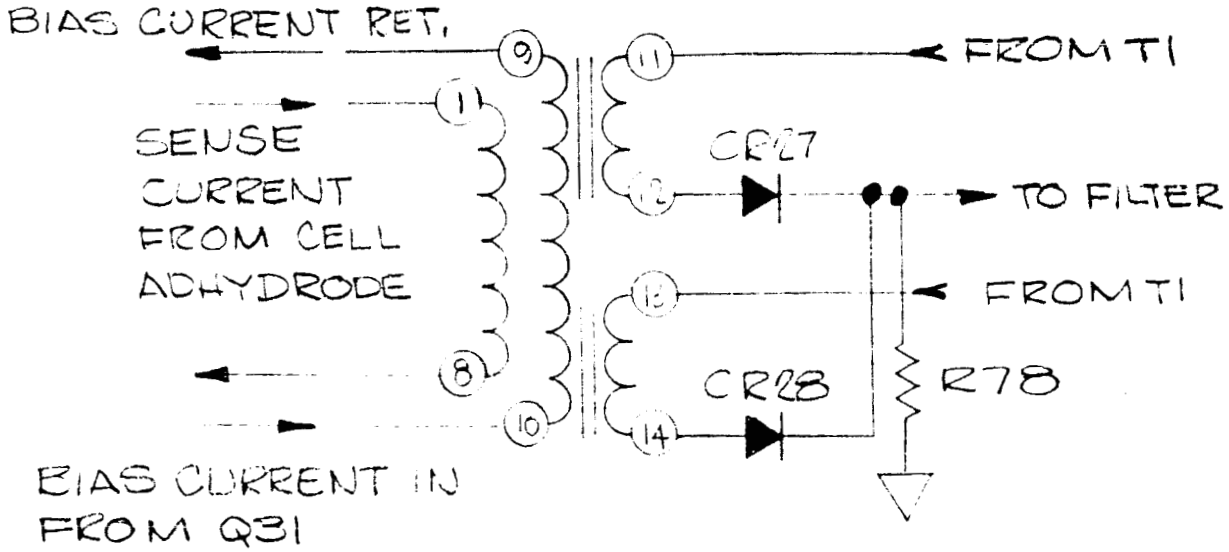


FIGURE 2-26. MAGNETIC AMPLIFIER SIMPLIFIED DIAGRAM.

c. The Filter shown in Figure 2-27 consists of an RC network and an emitter follower, which was added in order to make R large enough so that the action of the Magnetic Amplifier was not affected.

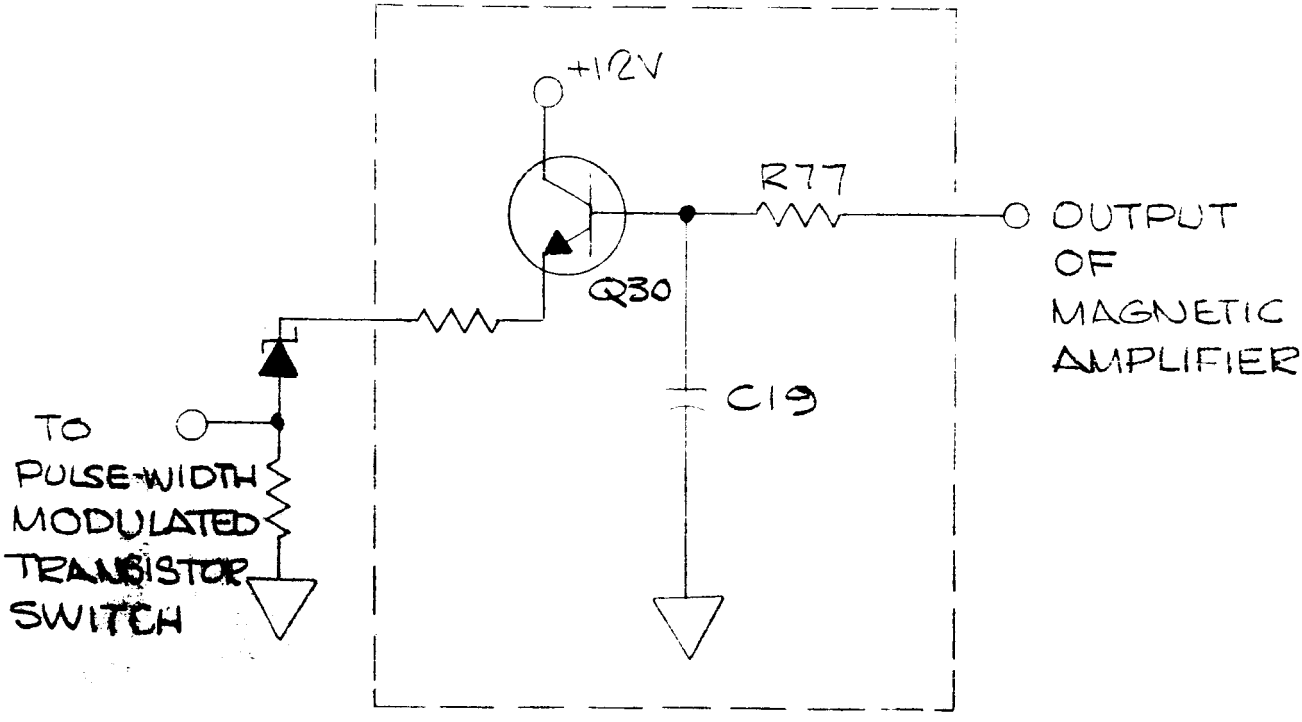


FIGURE 2-27. FILTER.

III. TEST DATA.

A. SYSTEM OPERATION MEASUREMENTS.*

1. Rustrak Recordings.

a. The Optimum Charging System can be operated in six different modes as follows:

Maximum Power Charging Controlled By:

(1) Signal from Ampere-Hour Meter

(2) Signal from Adhydrodes of battery cells

(3) Signal from either Ampere-Hour Meter or Adhydrodes

Taper Charging Controlled By:

(4) Signal from either Ampere-Hour Meter or Adhydrodes

(5) Signal from Adhydrodes of battery cells

(6) Signal from Ampere-Hour Meter

b. Figure 3-1 shows the plots recorded during the maximum power charging controlled by the signal from the Ampere-Hour Meter. The Solar Array Simulator was adjusted so that the Solar Array Simulator output was 21 volts. The current limiting point was 7.3 amperes. A 70 watt load was connected to the system to simulate the satellite load. The same input and load conditions apply to all test data recorded.

c. The charge portion of the State-Of-Charge plot on Figure 3-1 is approximately a straight line. The Battery current is constant since the maximum available power is constant at the Solar Array Simulator condition. There is little battery voltage change during the charge period. The Adhydrode voltage in the plot is generally a slant line upward because the cycling began with the cell fully charged and with the Adhydrode voltage at zero.

* Refer to Figure 3-20 for test setup.

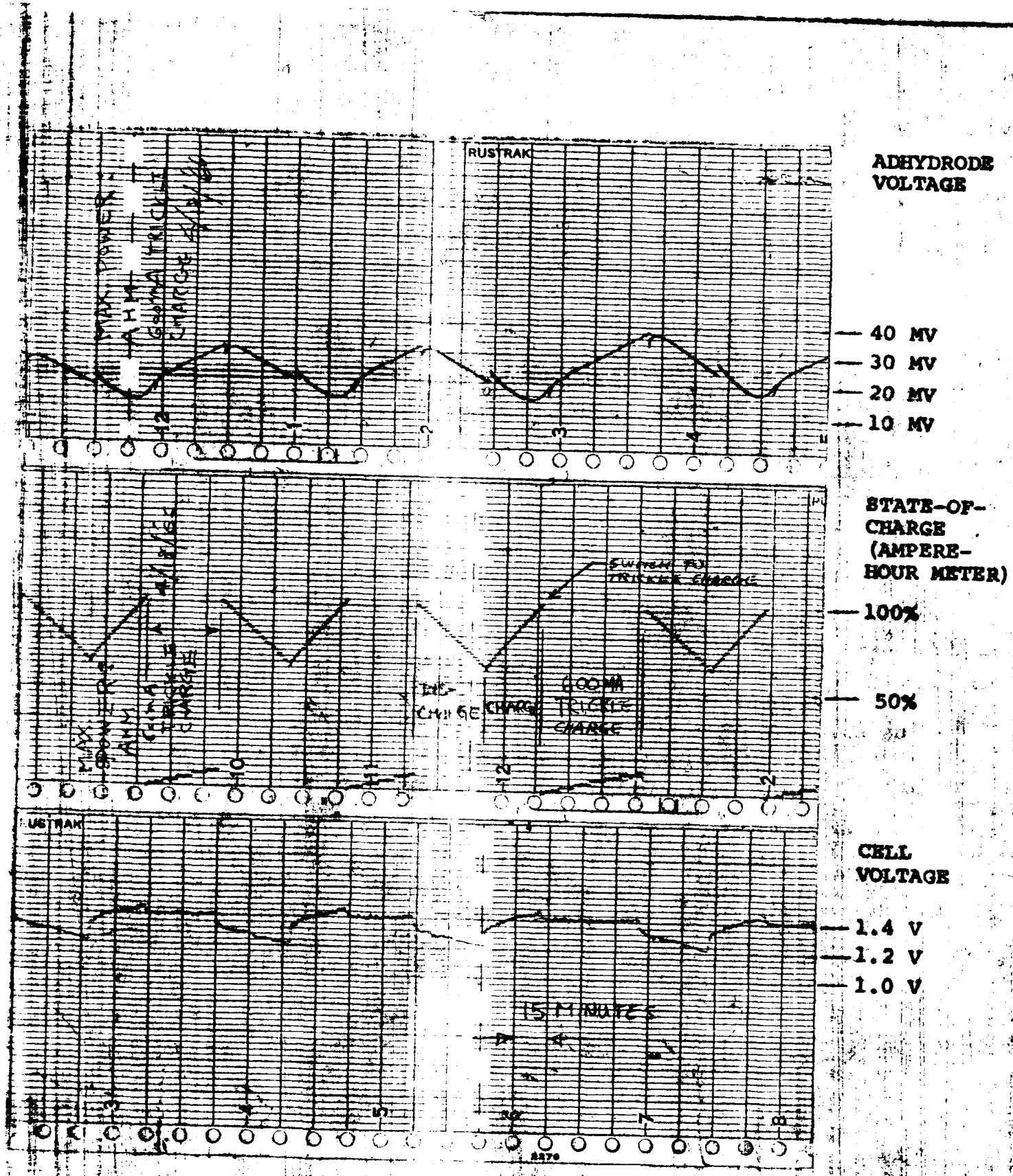


FIGURE 3-1. MAXIMUM POWER CHARGING CONTROLLED BY AMPERE-HOUR METER SIGNAL.

d. After many cycles, a steady-state condition was reached. In this condition the Adhydrode voltage variation was the same for all cycles. The Adhydrode voltage was about 15 MV at the point where the system switched to trickle charge at the command of the Ampere-Hour Meter. Figure 3-2 shows the system operation at the point where the Adhydrode voltage at 27 MV switches the system to trickle charge. The Ampere-Hour Meter in this condition indicates that the system should go into the trickle charge mode slightly sooner than it did.

e. If the switching voltage of the Adhydrode were reduced to about 15 MV, the Ampere-Hour Meter and the Adhydrode signal would each indicate the fully charged condition at about the same time.

f. Figure 3-3 shows the condition in which either the Ampere-Hour Meter signal or the Adhydrode signal, whichever comes first, switches the system to trickle charge. When the Adhydrode voltage is set to 27 MV for switching, the Ampere-Hour signal controls the charge mode.

g. In Figure 3-4 the charger is basically a pulse-width modulated regulator, which effects a taper charge. The Adhydrode voltage (set to switch the system at 27 MV) controls the charging mode rather than control by the Ampere-Hour Meter. This is in contrast with the Maximum Power Charging situation.

h. Figure 3-5 shows the plots recorded for a number of charge-discharge cycles when the taper charge is controlled by the Adhydrode signal. The Ampere-Hour Meter indicates that

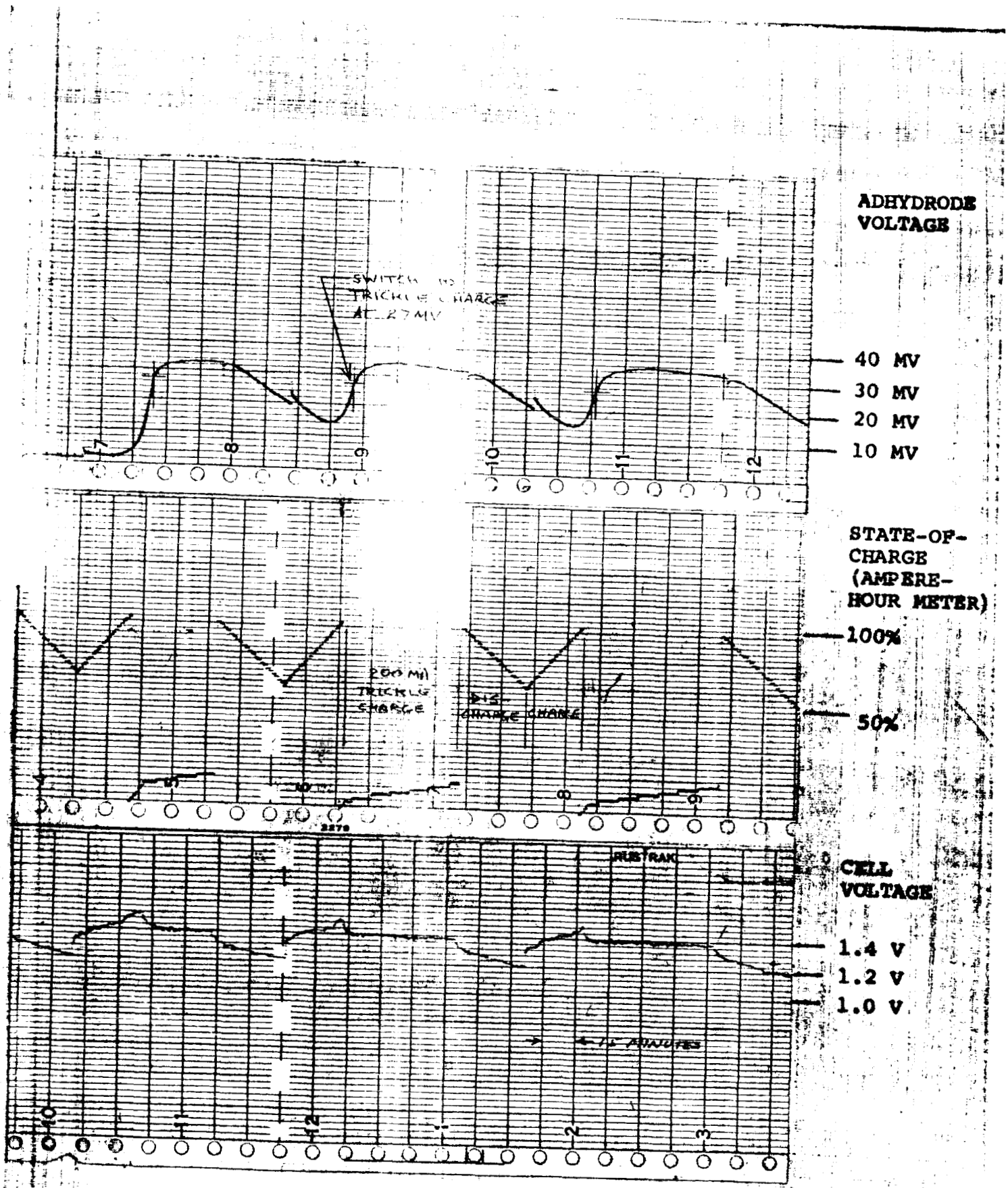


FIGURE 3-2. MAXIMUM POWER CHARGING CONTROLLED BY ADHYDRODE SIGNAL.

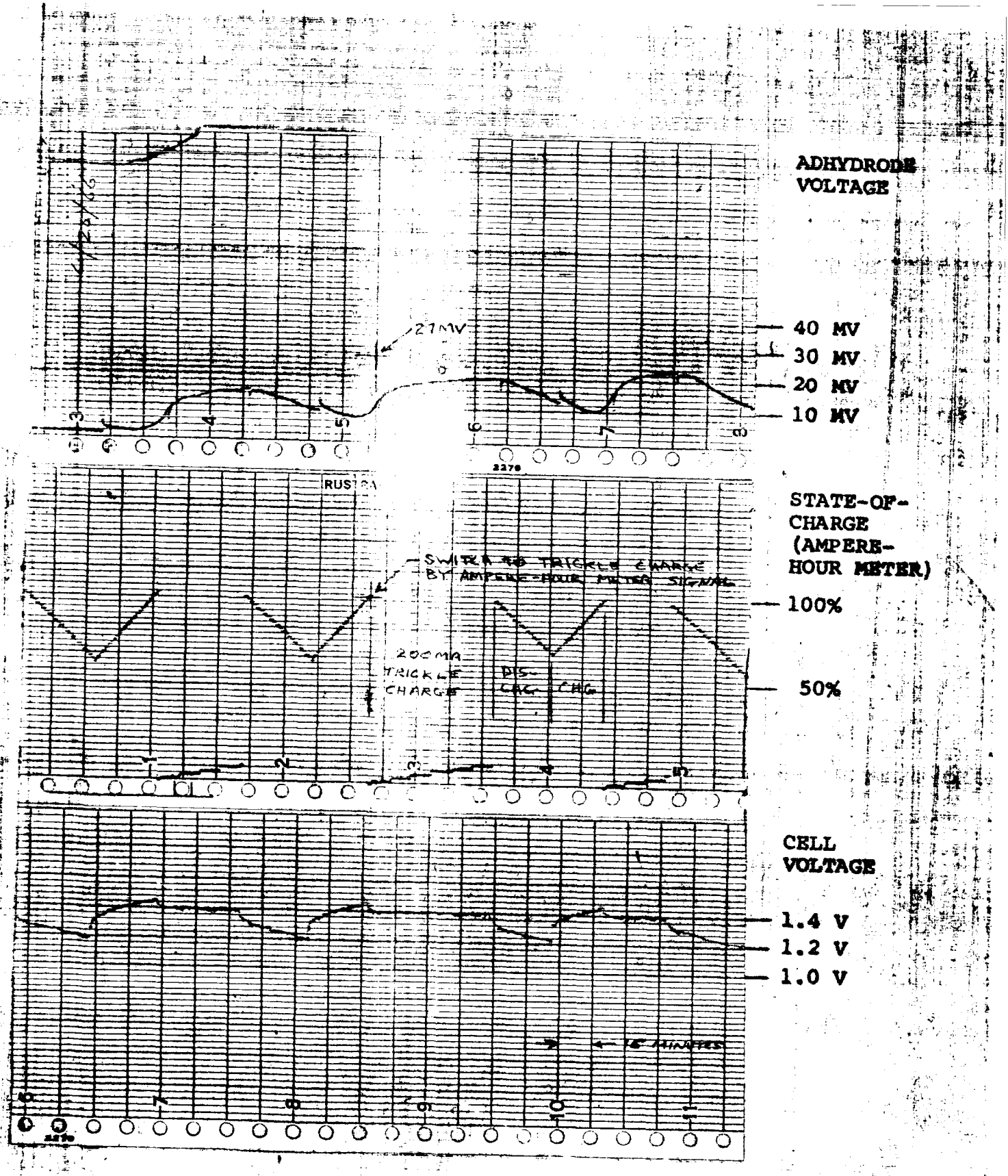


FIGURE 3-3. MAXIMUM POWER TRACKER CONTROLLED BY AMPERE-HOUR METER OR ADHYDRODE SIGNAL.

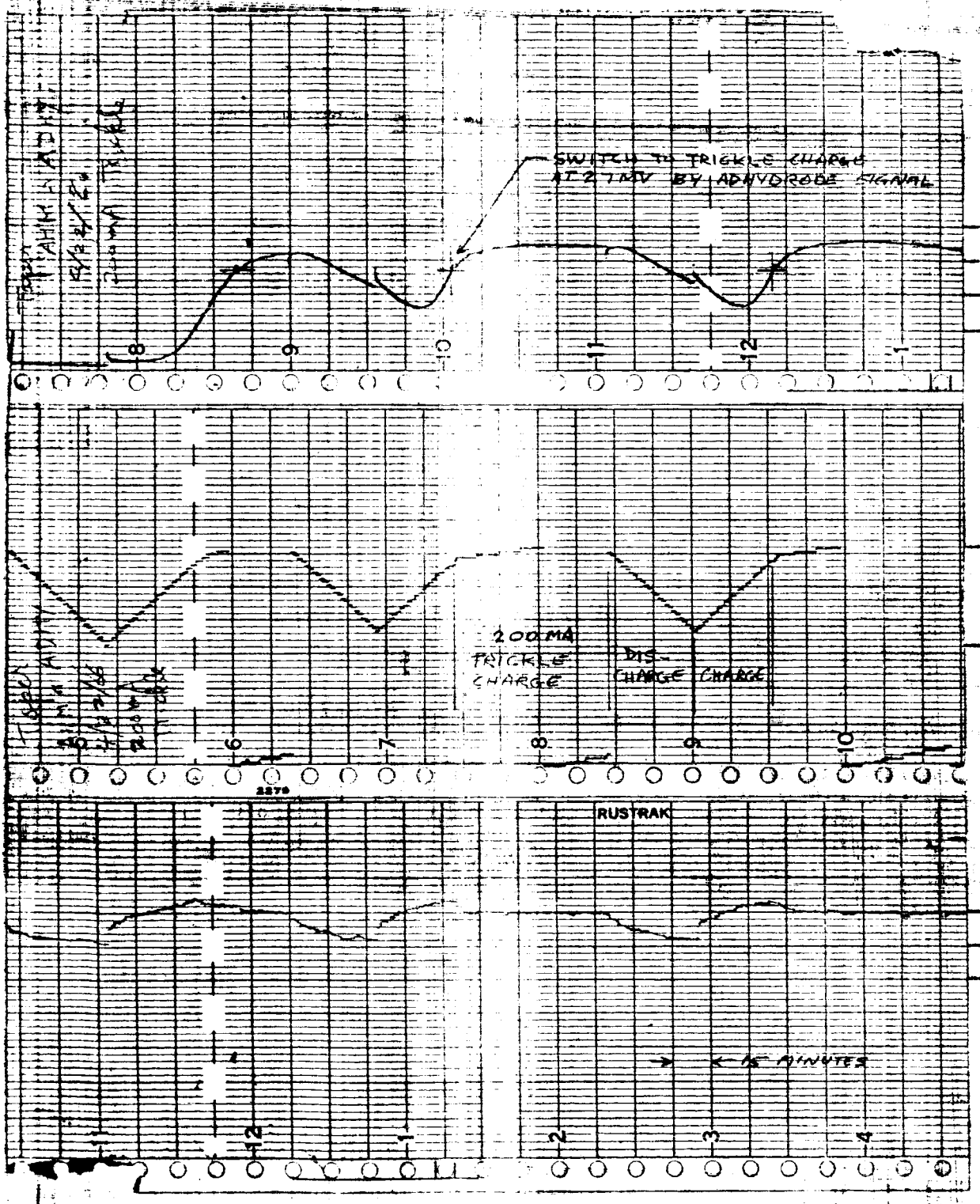


FIGURE 3-4. TAPER CHARGING CONTROLLED BY AMPERE-HOUR METER OR ADHYDRODE SIGNAL.

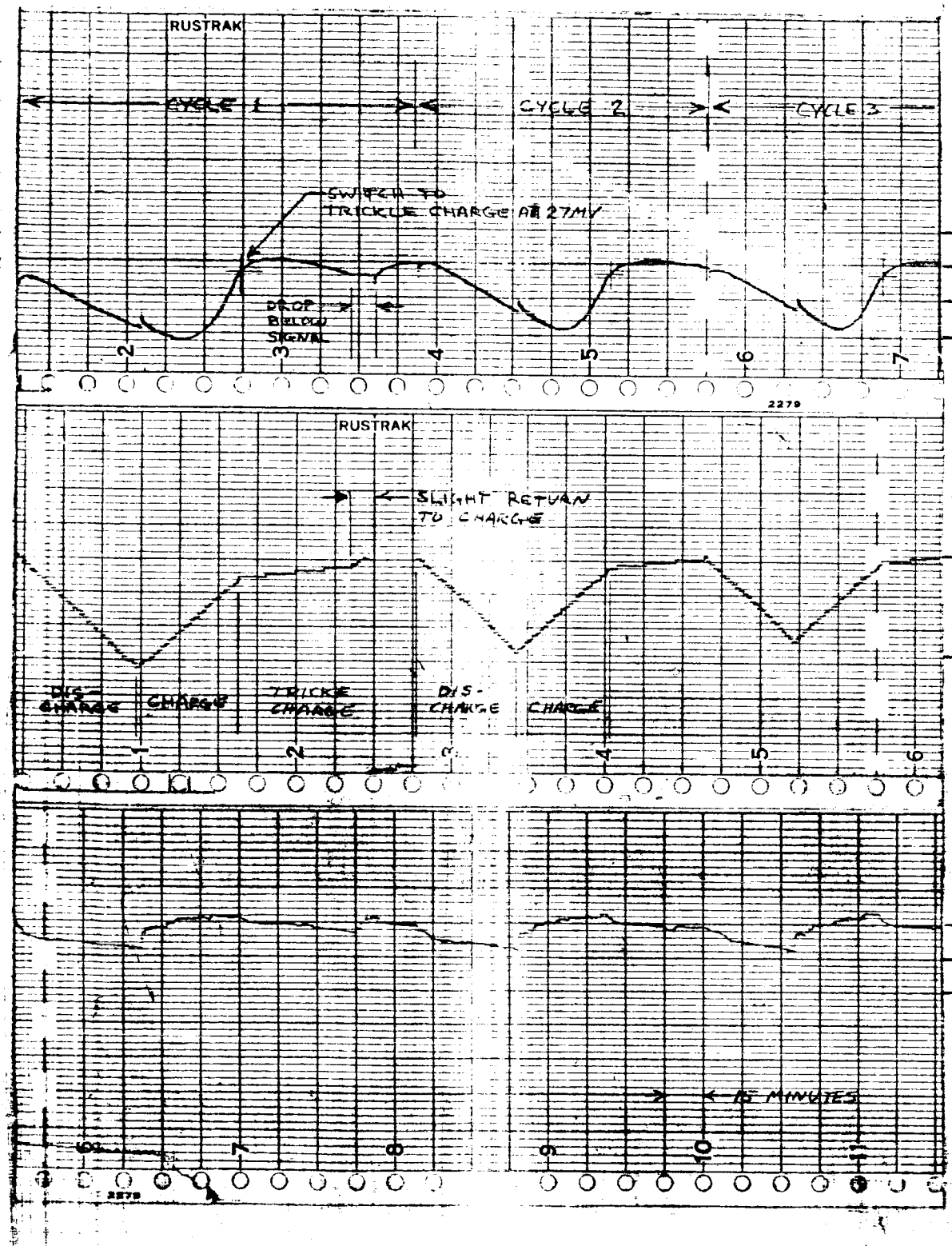


FIGURE 3-5. TAPER CHARGING CONTROLLED BY ADHYDRODE SIGNAL.

the switching operation to trickle charge by the Adhydrode signal is slightly fast, especially in the first cycle. However, in the second cycle the Ampere-Hour Meter and the Adhydrode voltage are in better agreement with the fully charged condition of the cell. The switching voltage of the Adhydrode should be increased slightly for complete agreement. Notice that at the end of the first cycle charging period the system returns to "charge" from "trickle charge" because the Adhydrode voltage dropped below the set switching level during the stand-period.

i. Figure 3-6 represents the last situation where the taper charging is controlled by the Ampere-Hour Meter signal.

j. From the chart recordings on Figures 3-1 and 3-5, with the Ampere-Hour Meter indicating that the cell is in the fully charged state, the Adhydrode voltages are approximately 15 MV and 30 MV for Maximum Power Charging and Taper Charging conditions respectively. The resistor value across the Adhydrode and the negative terminal was 1Ω.

B. BATTERY ADHYDRODE MEASUREMENTS.*

1. Cycles of Operation Versus Sense Voltage.

a. The Gulton cell VO6HSAD (cell with Adhydrode) was subjected to the following initial experiment: The Battery cells were tightly packed. No plastic guards were provided. The tests were performed at room temperature without cooling provisions. Figure 3-7 shows the results of the experiment.

(1) The Battery was reconditioned.

(2) Discharge at 6A for thirty minutes. 6A

* Refer to Figure 3-20 for test setup.

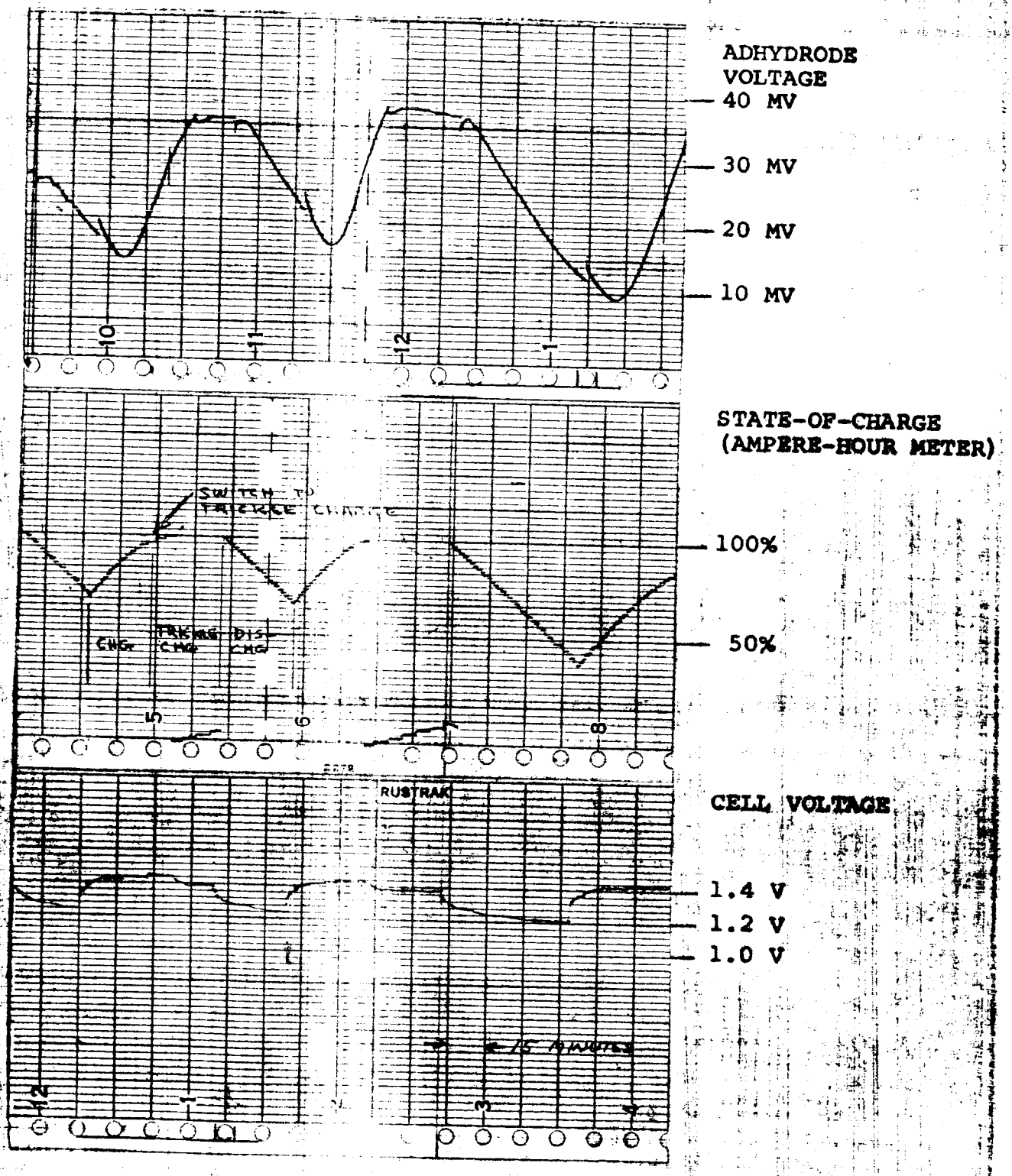


FIGURE 3-6. TAPER CHARGING CONTROLLED BY AMPERE-HOUR METER SIGNAL.

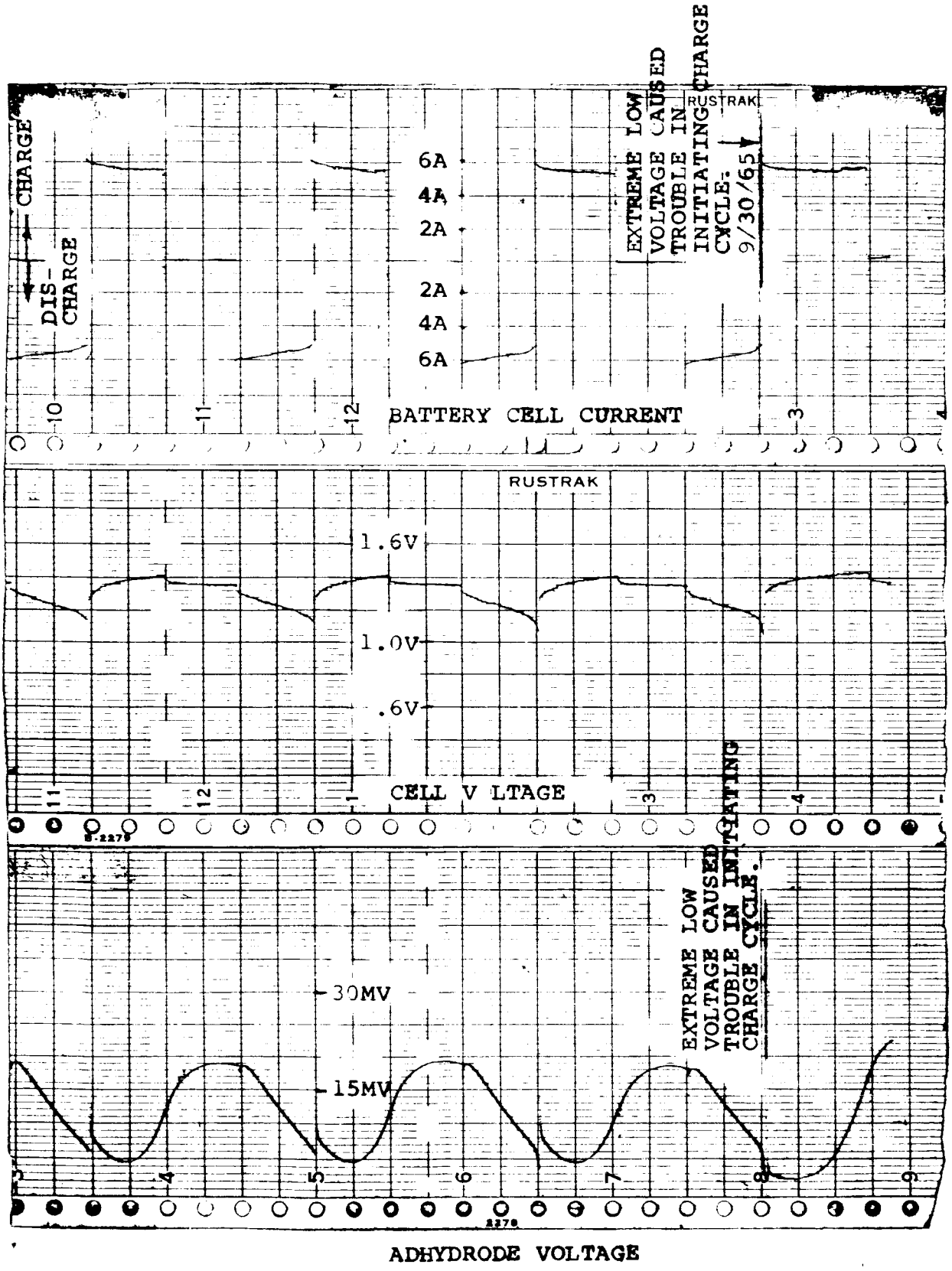


FIGURE 3-7. CHARGE-DISCHARGE CYCLES, INITIAL TEST, NO COOLING PROVISIONS.

charge until the Adhydrode voltage reached 12 MV (1Ω across Adhydrode) after which the charging current was shut off and the cell left on stand. After 17 cycles, the cell voltage at the end of discharge dropped to about one volt.

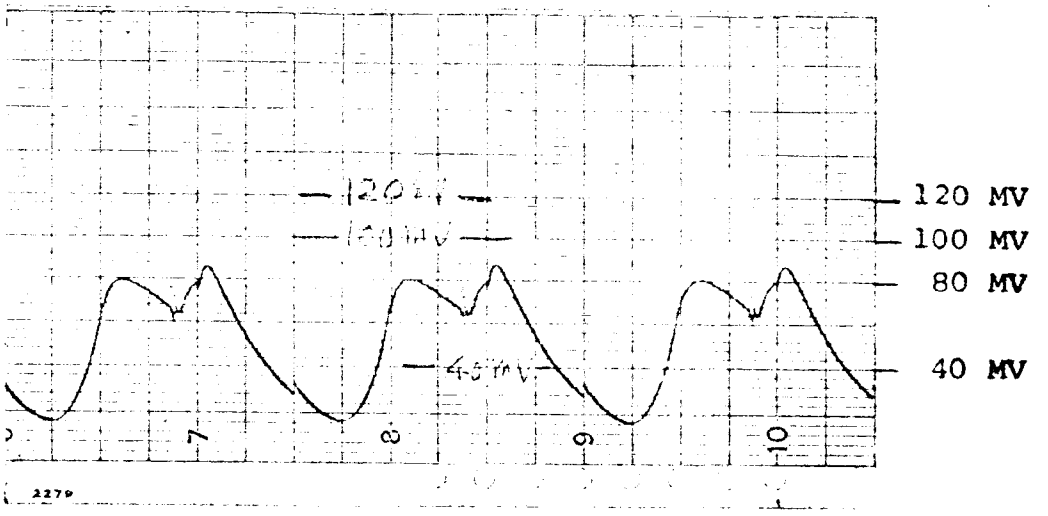
(3) The cell was left on stand until the Adhydrode voltage dropped to practically zero, then the charge-discharge cycle was initiated as in (2) except that the cell was disconnected from the charging source when the Adhydrode voltage reached 18 MV instead of 12 MV. After 22 cycles, the cell voltage reached approximately one volt.

(4) The cell was again left on stand until the Adhydrode voltage dropped to zero. Then the cycle was initiated as in (2) except the cell went from "charge" to "stand" when the Adhydrode voltage reached 28 MV. About 18 cycles were accumulated before the cell voltage dropped to about one volt.

b. In the next experiment, the battery pack of the Gulton 6 Ampere-Hour Adhydrode cells was subjected to charge-discharge cycles, first with the batteries fan cooled, and then without cooling. A typical portion of the recorder chart monitoring the Cell Voltage and the Adhydrode Voltage when the battery pack was fan cooled is shown on Figure 3-8, and when the battery pack was not cooled on Figure 3-9.

c. Following 100 cycles under the cooling condition, there was no indication of cell voltage drooping (see Figure 3-8).

ADHYDRODE VOLTAGE



CELL VOLTAGE

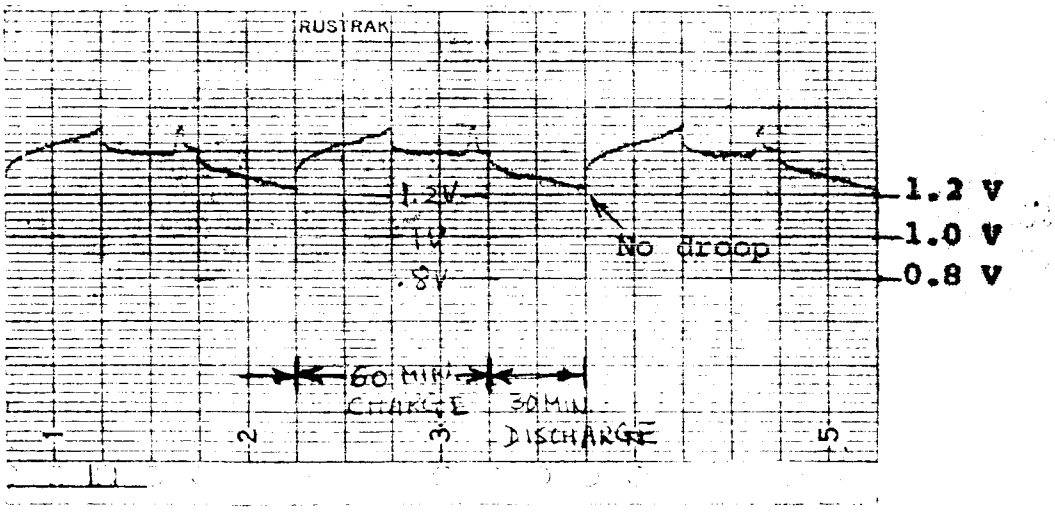


FIGURE 3-8. CHARGE-DISCHARGE CYCLES WITH BATTERIES FAN COOLED.

d. The fan was disconnected. After 30 cycles without cooling, there was cell voltage drooping as shown on Figure 3-9.

e. The battery cooling/non-cooling test conditions were both conducted with a 70 MV cutoff signal at the third electrode for the switching operation.

f. Conclusions reached were that without sufficient cooling provisions, the batteries would not accept a full charge during the charging period. They would therefore reach a severe energy depletion level before completion of a discharge period, thereby causing a voltage droop to occur.

2. Sense Voltages Versus Returned Amp-Hours.

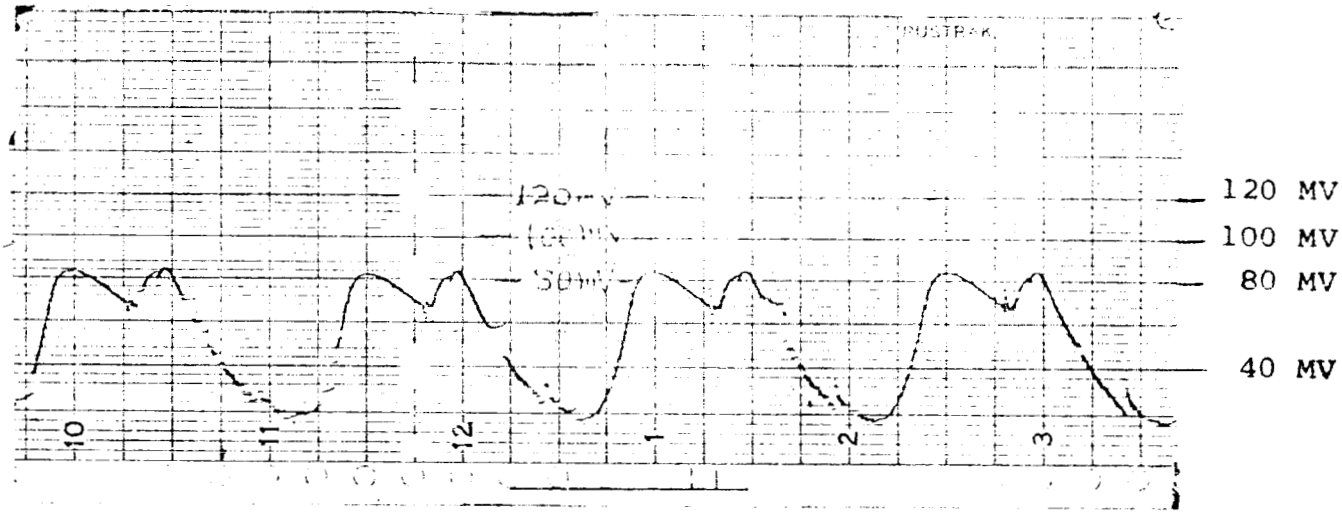
a. The following experiment was conducted on a Gulton 6 A-H Adhydrode Cell:

(1) The cell was discharged at a 6 ampere rate for 30 minutes and then charged at 6 amperes until the Adhydrode voltage was above 90 MV. A 1 ohm resistor was connected across the Adhydrode Cell for the test.

(2) The charge current was then turned off and the battery left to stand until the Adhydrode voltage dropped below 90 MV. The 6 ampere charge current was then reapplied (typically for 2 minutes) until the Adhydrode voltage was again above 90 MV. During the stand period, this action is somewhat similar to trickle charging.

b. The described procedure continued for about 140 cycles; then the cell was discharged to 1 volt and the capacity measured. The capacity of the cell was 3.35 ampere hours. Figure 3-10 is a portion of the chart recorded during the test.

ADHYDRODE VOLTAGE



CELL VOLTAGE

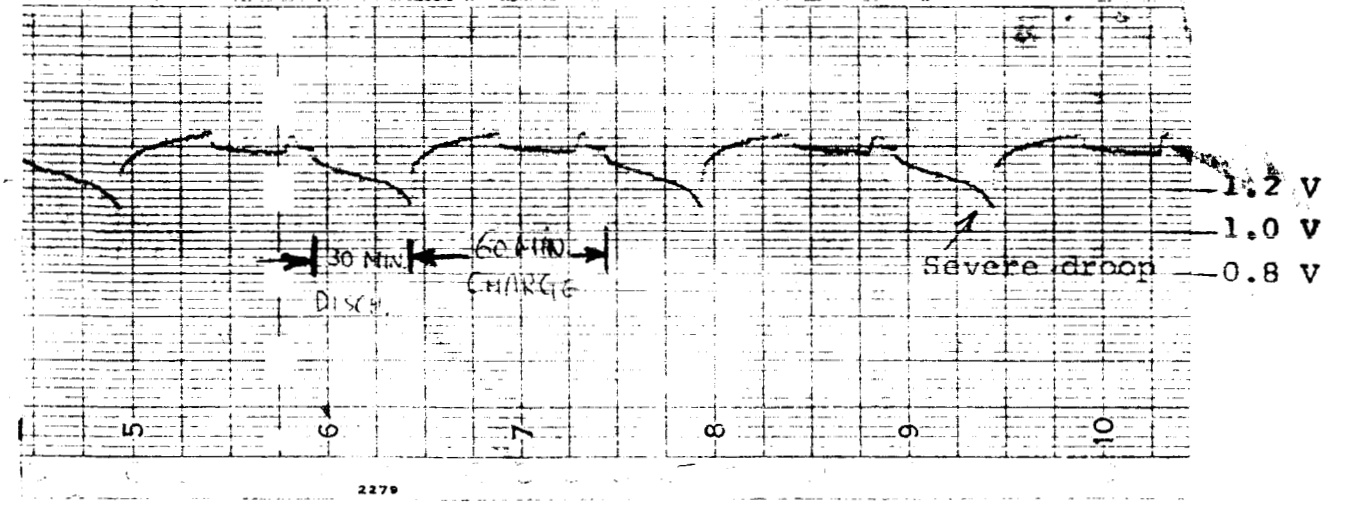


FIGURE 3-9. CHARGE-DISCHARGE CYCLES WITHOUT BATTERIES FAN COOLED.

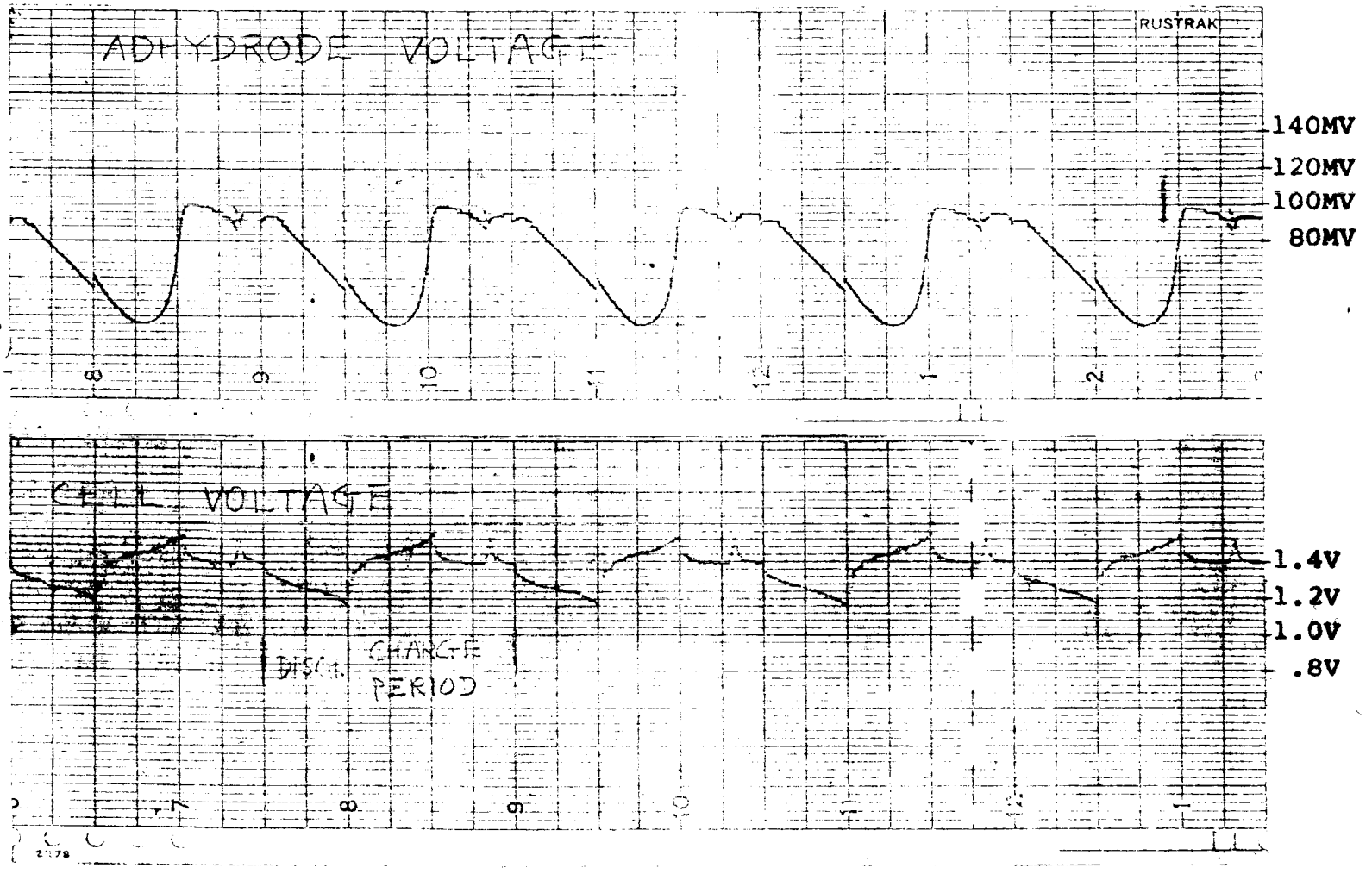


FIGURE 3-10. PORTION OF CHART RECORDED TO DETERMINE RETURNED AMP-HOURS.

C. OPTIMUM CONTROL MEASUREMENTS TRACKING ACCURACY*

1. Performance With Solar Array Simulator Variation

In this experiment the characteristics of the Solar Array Simulator were varied from 16 to 29 volts and limiting current from 5.9 amps to 9.1 amps (see Figure 3-11 for maximum power of Solar Array Simulator). Loads were set at 70 watts except for the condition of the lowest Solar Array Simulator voltage where the load was set at 18 watts. Table I is the tracking accuracy summary of results at room, low and high temperatures with the Solar Array Simulator voltage and current varied. Figures 3-12, 3-13, and 3-14 are the tracking accuracy summary of results at room, low and high temperature with the Solar Array Simulator at a constant 21 volts and current at 7 amps.

* Tracking Accuracy is measured in % utilization, the ratio of the maximum demand to the rated capacity. Refer to Figure 3-20 for test setup.

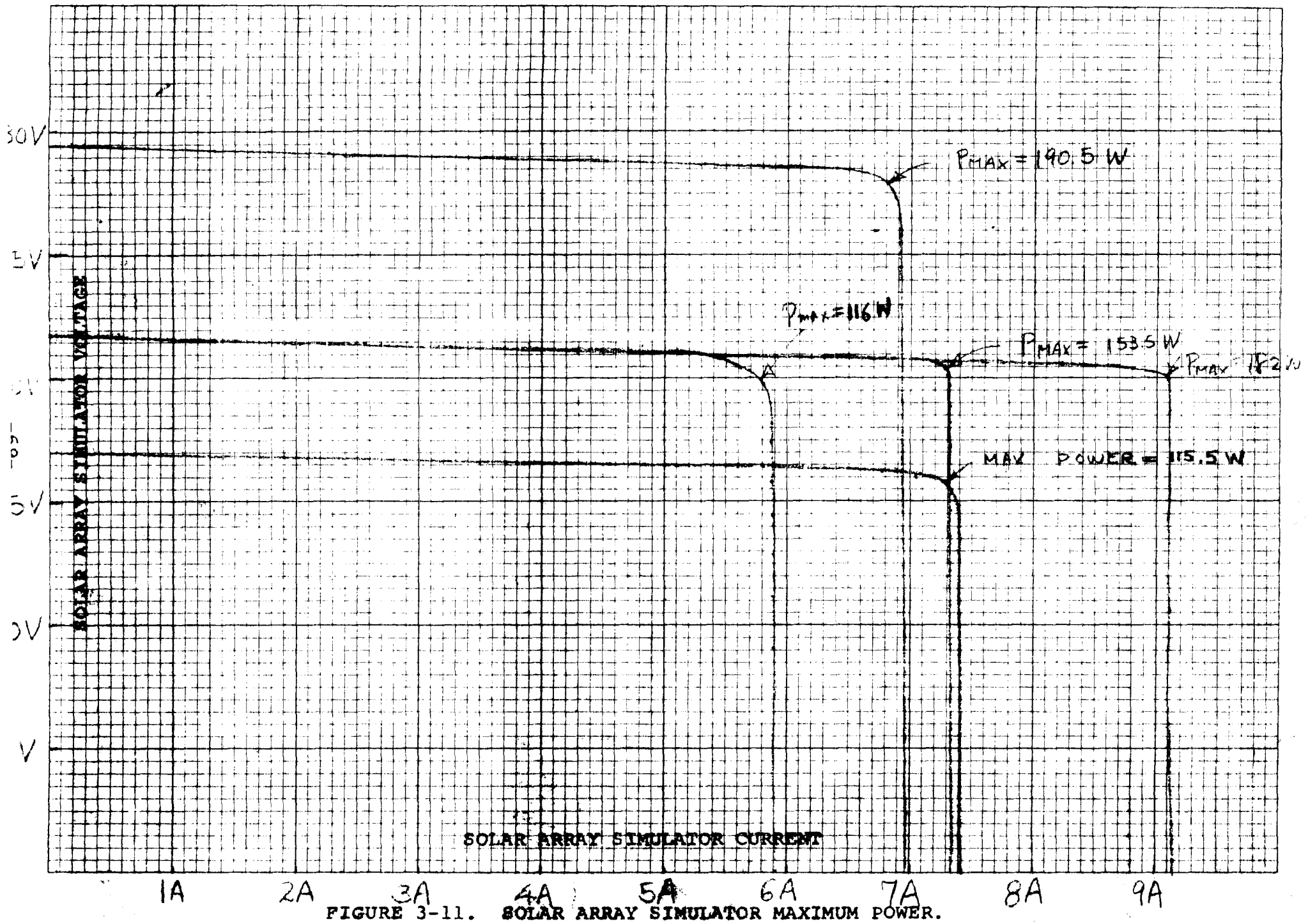


FIGURE 3-11. SOLAR ARRAY SIMULATOR MAXIMUM POWER.

ROOM TEMPERATURE

Variation of Array Voltage (Array Current Approximately 7 Amps)

Array Voltage (VDC)	Max. Power Point of Array Simulator	Output Power of Array Simulator	% Utilization
16	117	109	93.2
21	150	146	97.5
29	191	188	98.4
LOW TEMPERATURE 0°C			
16	117	106	94.8
21	150	143	95.3
29	191	186	97.4
HIGH TEMPERATURE 50°C			
16	117	110	94
21	150	142	94.7
29	191	184	96.3

ROOM TEMPERATURE

Variation of Array Current (Array Voltage Approximately 21 Volts)

Array Current (Amps)	Max. Power Point of Array Simulator	Output Power of Array Simulator	% Utilization
5.9	116	113	97.4
7.3	150	146	97.3
9.1	184	181	98.3
LOW TEMPERATURE 0°C			
5.9	116	110	94.8
7.3	150	143	95.3
9.1	184	175	95.1
HIGH TEMPERATURE 50°C			
5.9	116	112	96.5
7.3	150	142	94.7
9.1	184	175	95.1

TABLE I. TRACKING ACCURACY RESULTS AT ROOM, LOW, AND HIGH TEMPERATURES, ARRAY VOLTAGE AND CURRENT VARIED.

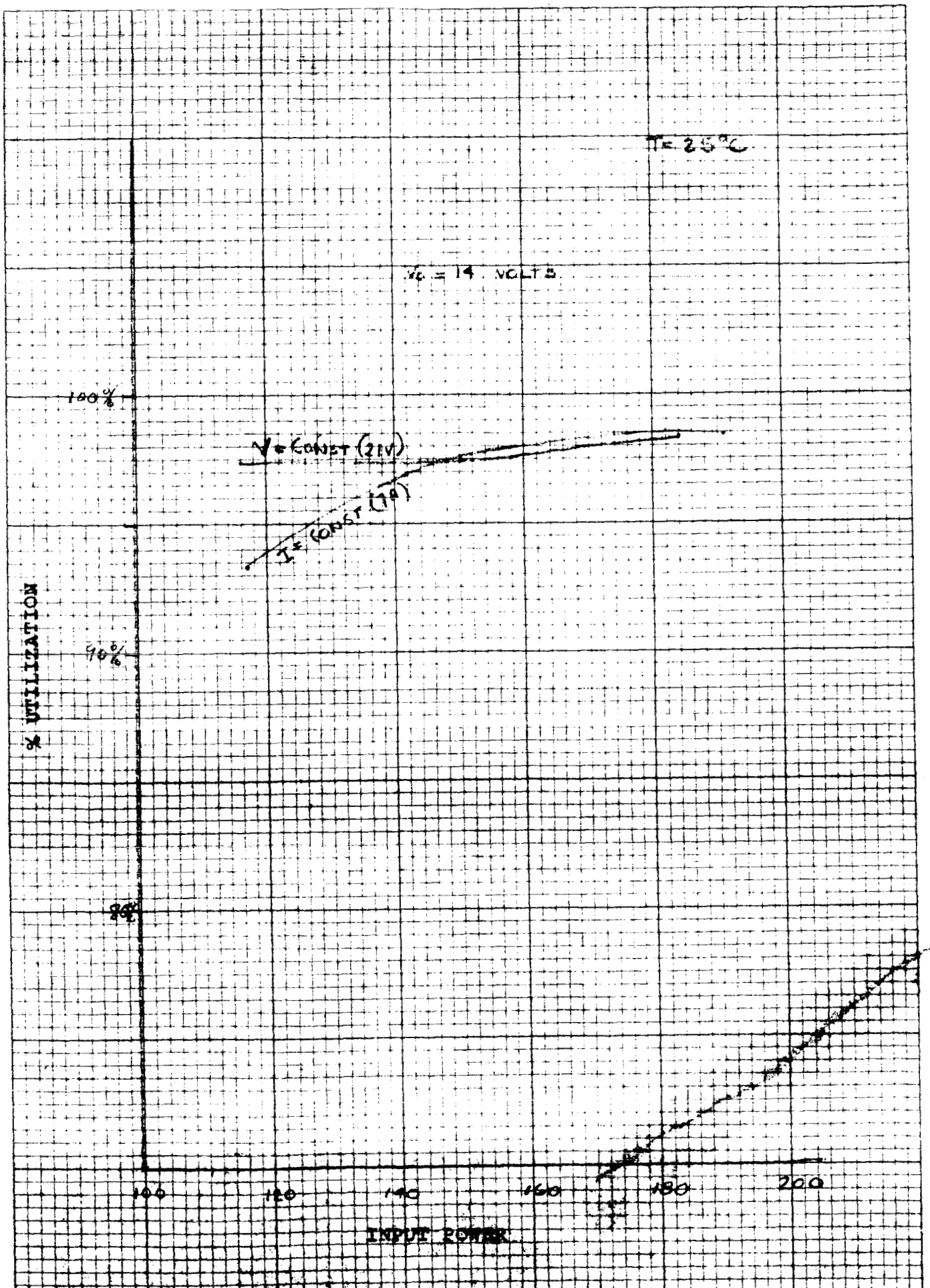


FIGURE 3-12. TRACKING ACCURACY RESULTS AT AMBIENT TEMPERATURE, ARRAY VOLTAGE AND CURRENT CONSTANT.

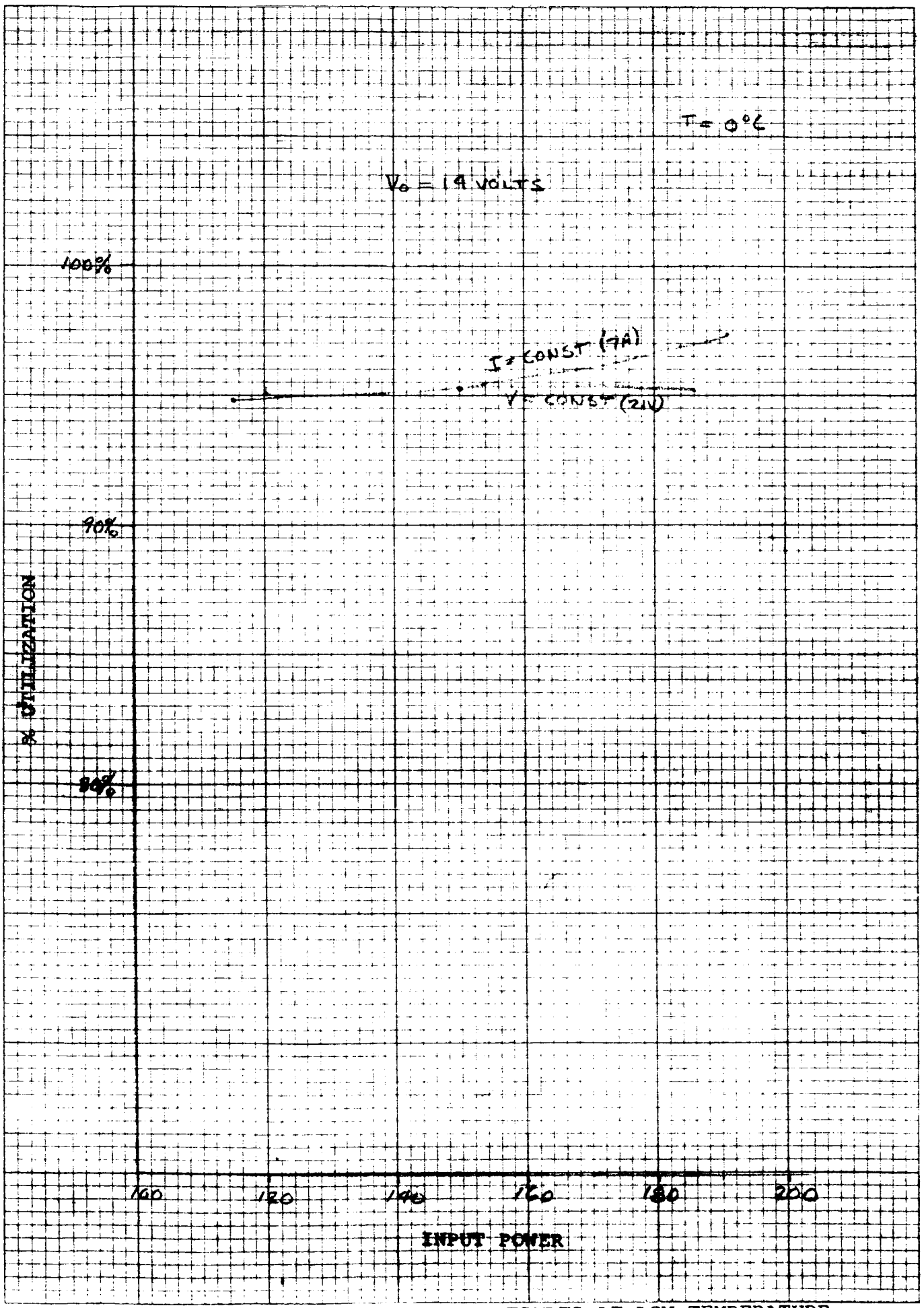


FIGURE 3-13. TRACKING ACCURACY RESULTS AT LOW TEMPERATURE, ARRAY VOLTAGE AND CURRENT CONSTANT.

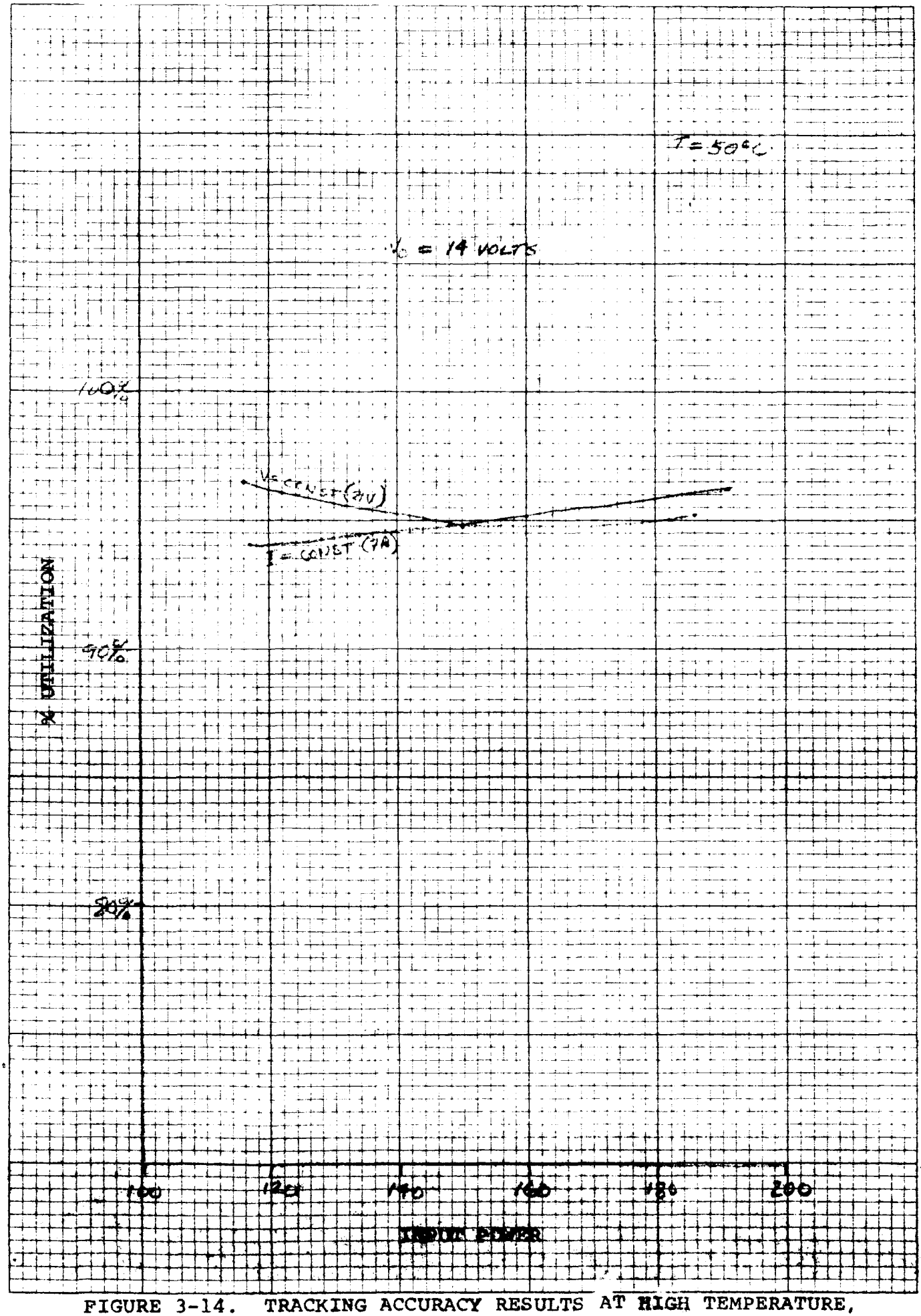


FIGURE 3-14. TRACKING ACCURACY RESULTS AT HIGH TEMPERATURE, ARRAY VOLTAGE AND CURRENT CONSTANT.

2. Performance With Load Variation

In this experiment the Solar Array Simulator was set at nominal value (21 volts and 7.3 amperes limiting) and at room temperature. The maximum power point of the Solar Array Simulator in this condition was 150 watts. The following results show the data obtained on tracking accuracy when the load is varied.

Load Current (Amps)	Output Power of Array Simulator (Watts)	% Utilization
.74	142	94.4
1.96	140	93.5
3.54	146	97.3
4.12	144	96.2

3. Performance With Battery Voltage Variation

In this experiment the Solar Array Simulator was set at nominal value (21 volts and 7.3 amperes limiting). The maximum power point of the Solar Array Simulator in this condition was 150 watts. The load was set at the nominal value of 70 watts. The data below summarizes the tracking accuracy when the battery voltage is varied.

Battery Voltage (VDC)	Output Power of Array Simulator (Watts)	% Utilization
13.5	147	97.6
14.2	146	97.3
15	147	97.6

4. Response to Step Load Change and Step Input Change

The photograph, Figure 3-15, shows the battery current change of 2 amperes due to step load change (decrease of load). The battery current reaches the final value in approximately 4 seconds.

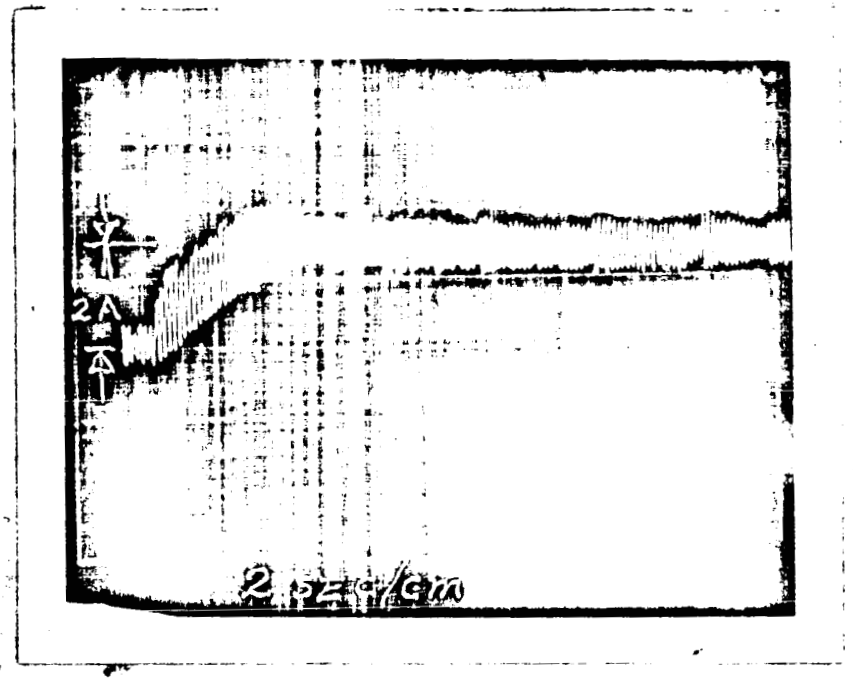


FIGURE 3-15. BATTERY CURRENT CHANGE DUE TO STEP LOAD CHANGE.

The settling time of the Maximum Power Tracker to the step input change was as follows: (The Solar Array Simulator is applied instantaneously to the Maximum Power Tracker.)

Solar Array Characteristic	Settling Time
7 amps - 16V	15 seconds
7 amps - 21V	8 seconds
7 amps - 30V	12 seconds
21V - 6 amps	8 seconds
21V - 7 amps	8 seconds
21V - 10 amps	9 seconds

The load was at the nominal value of 70 watts.

5. Response to AC Loads on Solar Array Simulator

The following data shows the result of the measurements of the Solar Array Simulator average current and average voltage when the load was varied dynamically. The test conditions were:

Array: At nominal characteristic of 21 volts at 7.3 ampere current limiting.

Load: Nominal value of 70 watts.

Array Output Without Load Disturbance:
7.17 amps at 20.65 volts.

Load Variation: 13.5 watts peak-to-peak
(60 - 73.5 watts).

Frequency (CPS)	Average Current (Amps)	Average Voltage (VDC)
1	7.15	20.5
5	7.17	20.5
10	7.17	20.43
30	7.18	20.45
50	7.17	20.45
100	7.1	20.53
200	7.02	20.58
300	7.05	20.55
500	7.19	20.2
1000	7.18	20.2

D. POWER LOSS MEASUREMENTS*

1. Shunt Losses

a. Ampere-Hour Meter: 400 MW

b. Maximum Power Tracker: Typically 1.3 watts.

c. Charge Control Regulator: 100 MW for taper charge and negligible for maximum power charge.

d. Adhydrode Sense and Control Circuit: 240 MW

e. Load Pulse Width Regulator: 100 MW

The Maximum Power Tracker shunt loss varies somewhat with the Solar Array Simulator voltage as shown in Figure 3-16.

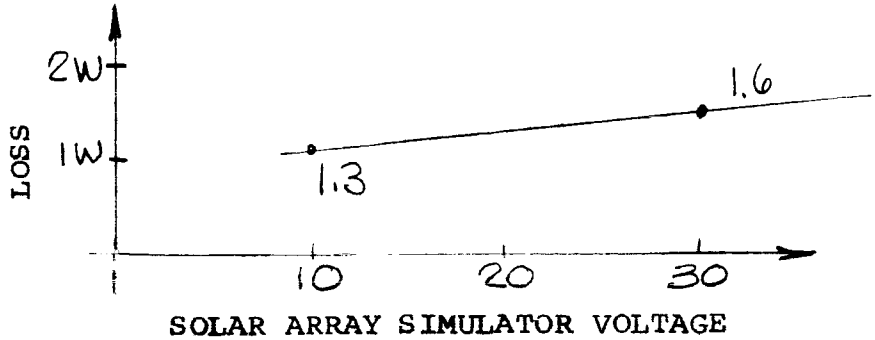


FIGURE 3-16. MAXIMUM POWER TRACKER SHUNT LOSS VARIATIONS WITH SOLAR ARRAY SIMULATOR VOLTAGE.

* Refer to Figure 3-20 for test setup.

2. Load Dependent Series Losses

The Charger and Load Regulator dissipate approximately 8% of the power handled. The following is the data taken on the transistor switch of the Maximum Power Tracker:

Conditions of Solar Array Simulator	% Efficiency of Transistor Switch
16V at 7 amps limiting	90.8
21V at 7 amps limiting	93.4
29V at 7 amps limiting	91.1
20V at 5.9 amps limiting	91.2
20V at 7.3 amps limiting	93.4
20V at 9.1 amps limiting	92.2

E. LIFE TEST

The life test program of the primary contract began on December 28, 1964 and was originally scheduled to conclude on April 10, 1965 but was continued throughout the duration of the primary and "add-on" contracts.

The life test program was conducted in the following manner using the NASA and Engineered Magnetics breadboards of the Ampere-Hour Meter Taper Charge System:

1. The capacity of a fully charged battery was measured with an Engineered Magnetics, Laboratory Type, Ampere-Hour Meter (Model EMAM104).
2. The battery was then discharged to an output level of 1 volt per cell. The battery capacity was then re-measured.
3. Using an external constant current source the battery was re-charged and then connected to the system breadboard and operated for one week.
4. The process was continuously repeated, and approximately 2840 Charge-Discharge cycles had been run on the battery at the end of the study program.

5. Figure 3-17 is a diagram of the setup used during the life test.

Typical recorder plots obtained during the life test of the NASA and Engineered Magnetics breadboards are presented in Figures 3-18 and 3-19. The following information is obtained from the recorder plots.

Battery Voltage

At:	Start of Discharge	13.2 VDC
	End of Discharge	11.6 VDC
	Start of Charge	13.2 VDC
	Full Charge	14.7 VDC
	Trickle Charge	14.3 VDC

Battery Current

Trickle Charge Current	.8 to 1.0 ampere
Recharge-Discharge Ampere-Hours	130%
Time to Full Charge	45 minutes
Current, Region B (Current Limited Charge Portion)	6.4 amperes
Taper Charge Current	6.0 to 2.0 amperes

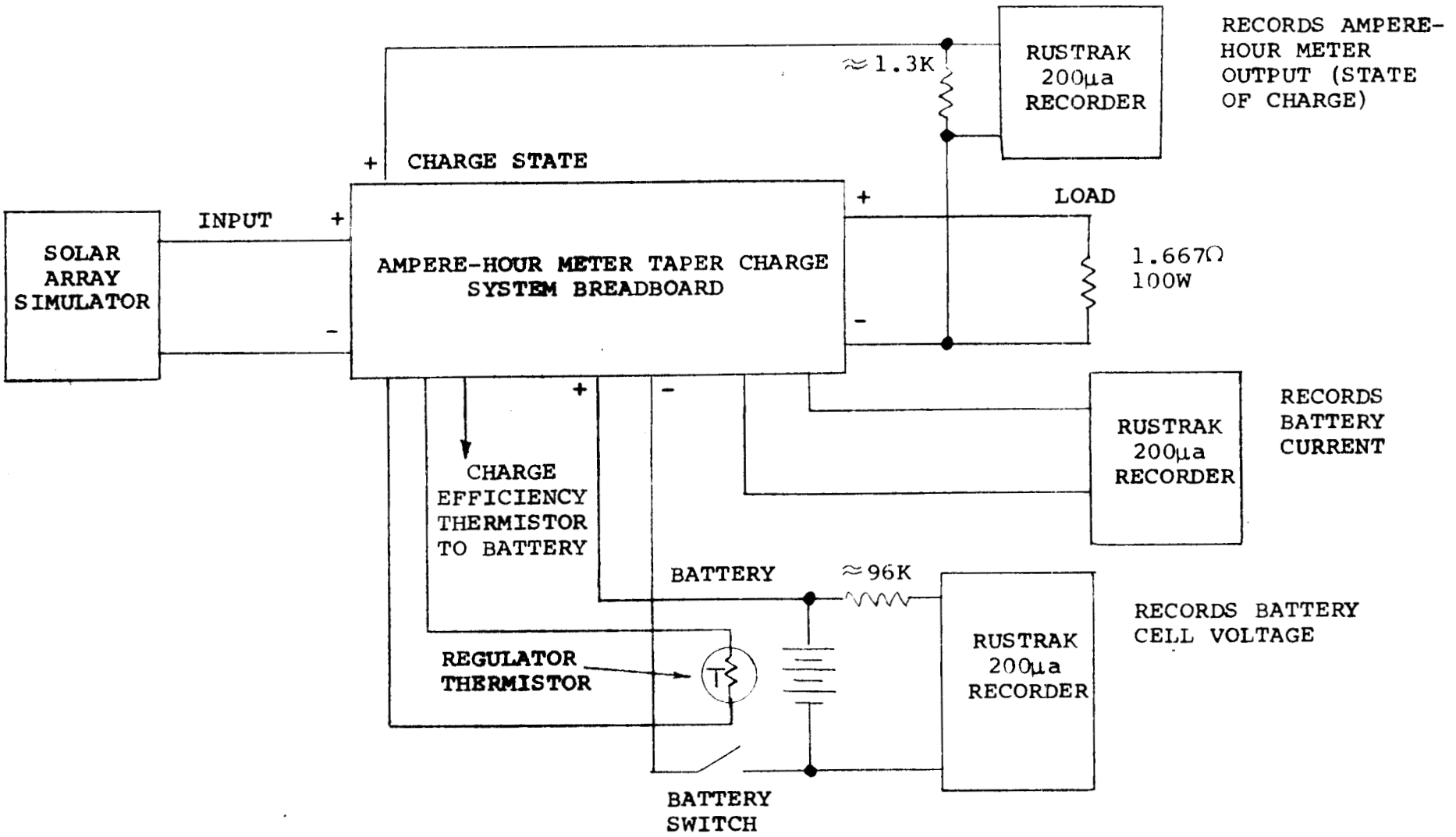
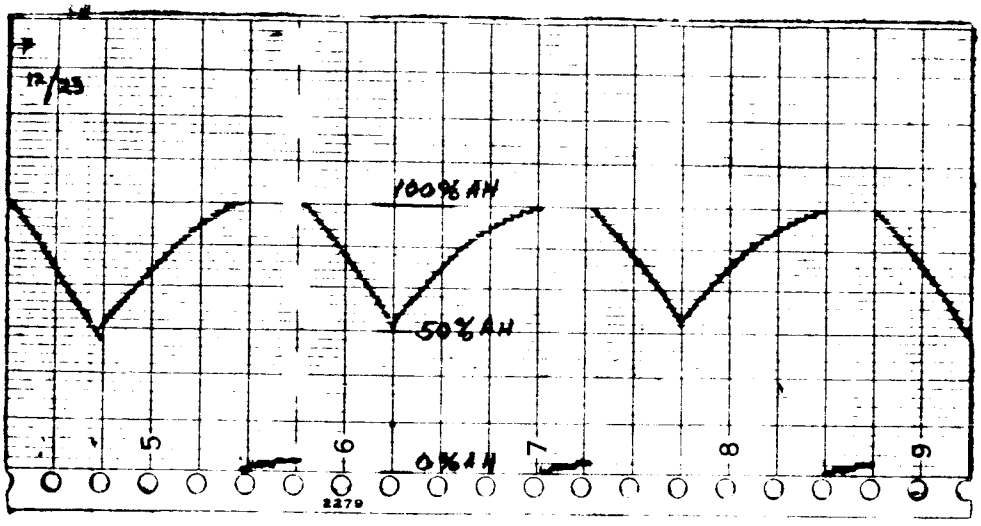
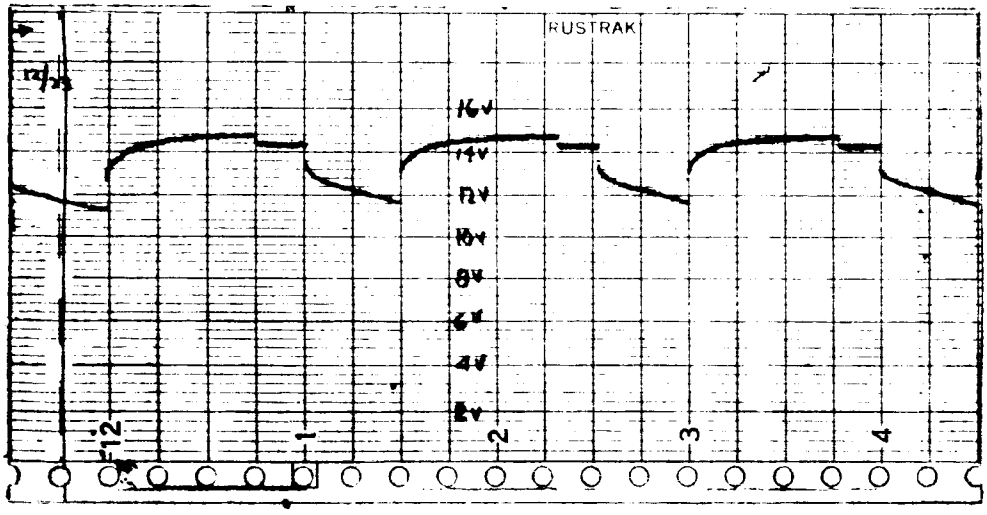


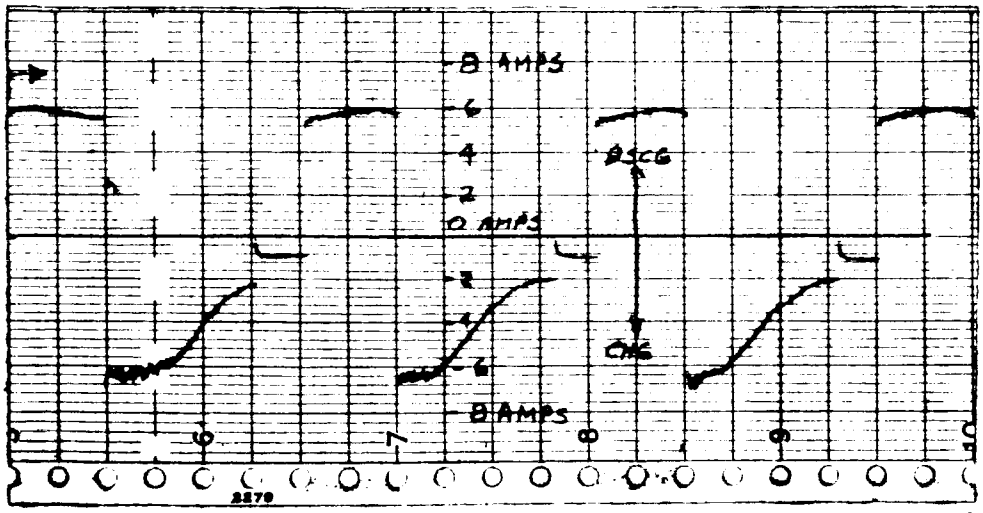
FIGURE 3-17. LIFE TEST SETUP.



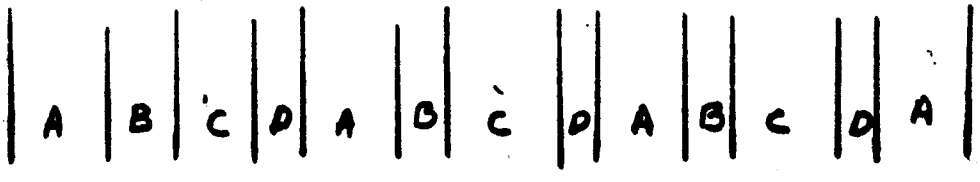
BATTERY AMPERE HOURS (READ ON CHARGE CONTROL A-H METER).



BATTERY VOLTAGE

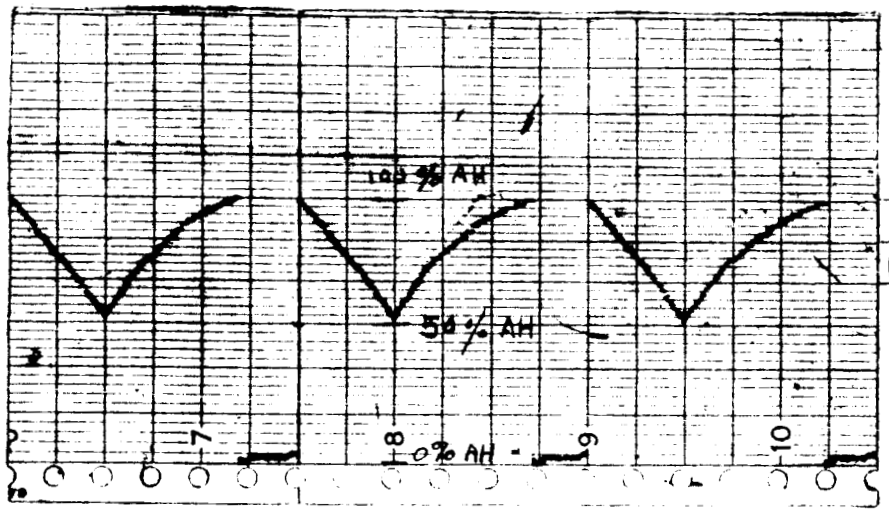


BATTERY CURRENT

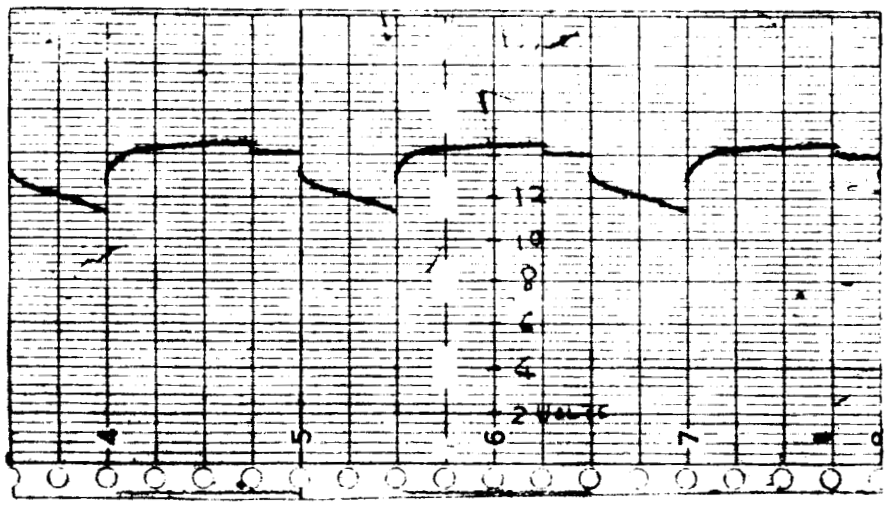


REGION A: DISCHARGE.
REGION B: CURRENT LIMITED CHARGE.
REGION C: TAPER CHARGE.
REGION D: TRICKLE CHARGE.

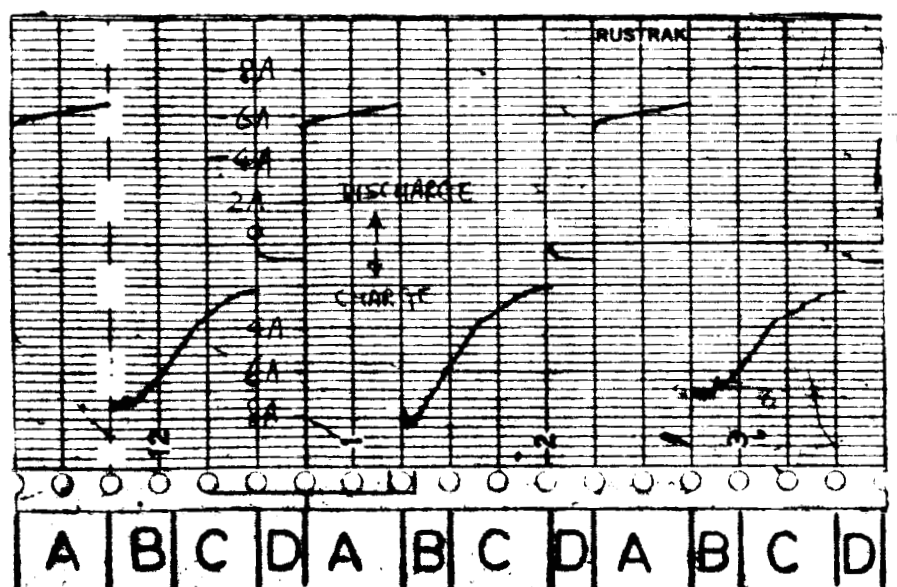
FIGURE 3-18. LIFE TEST RECORDER PLOTS, NASA BREADBOARD.



BATTERY STATE OF CHARGE



BATTERY VOLTAGE



BATTERY CURRENT

REGION A: DISCHARGE.
REGION B: CURRENT LIMITED CHARGE.
REGION C: TAPER CHARGE.
REGION D: TRICKLE CHARGE.

FIGURE 3-19. LIFE TEST RECORDER PLOTS, ENGINEERED MAGNETICS BREADBOARD.

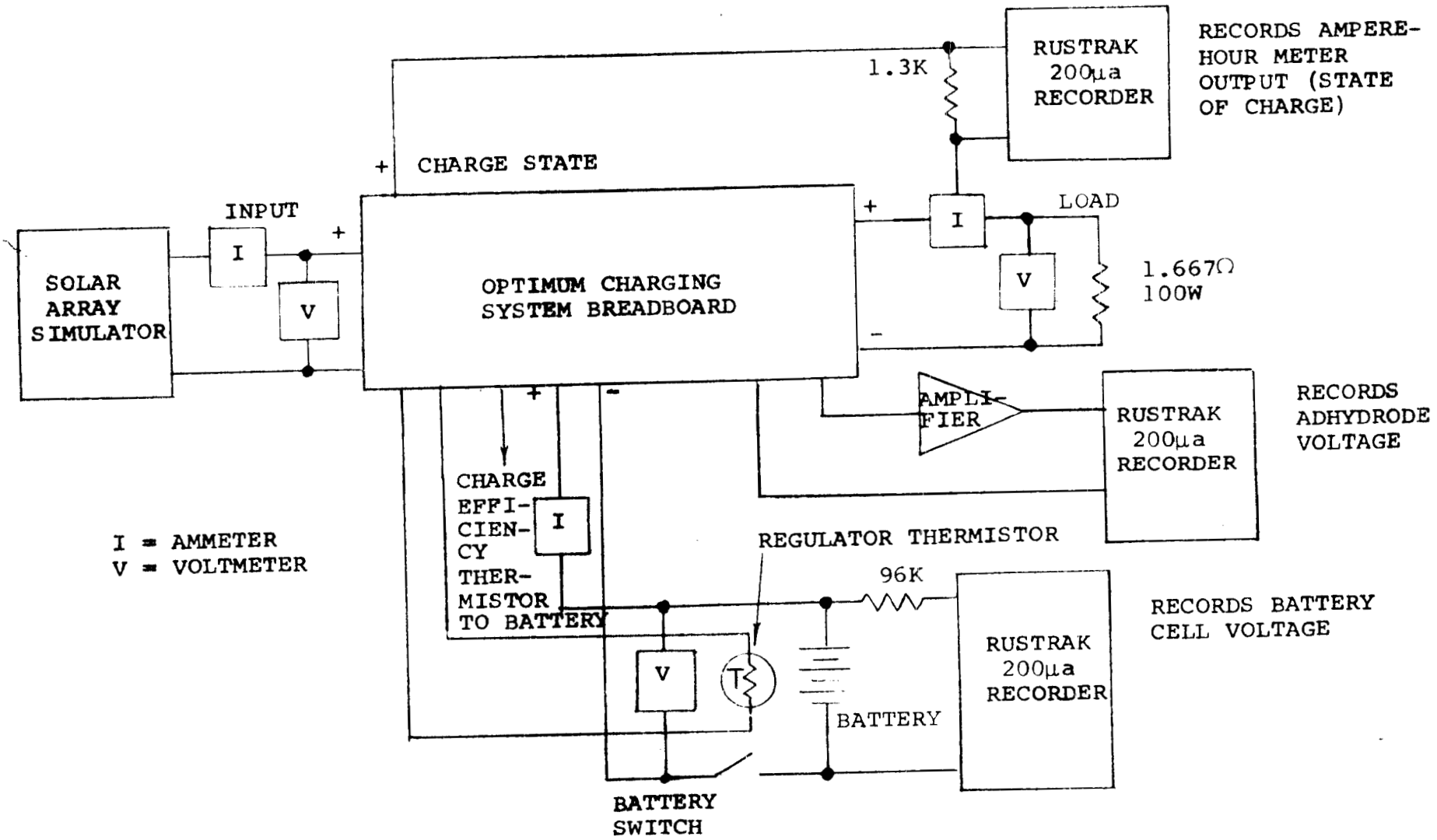


FIGURE 3-20. OPTIMUM CHARGING SYSTEM TEST SETUP FOR SYSTEM OPERATION, BATTERY ADHYDRODE, TRACKING ACCURACY, AND POWER LOSS MEASUREMENTS.

IV. ANALYSIS AND CONCLUSIONS

During the course of the study program, various electronic circuits were developed in addition to adapting previously designed circuits for use in satellite power systems. The purpose of this section of the report is to summarize these accomplishments and to show their relationship (conclusion) to an Optimum Charging System. In order to do this, Section IV is divided into three parts:

A. Description of circuits and techniques that were developed.

B. Analysis of a typical satellite power system.

C. Design of a specific satellite power system using the techniques developed.

A. DESCRIPTION OF CIRCUITS AND TECHNIQUES THAT WERE DEVELOPED

The following control components were developed:

1. Adaptation of high efficiency bucking regulators for use as:
   a) Load Pulse-Width Regulator.
   b) Taper charge battery regulator (Charge Control Regulator used in Ampere-Hour Meter Taper Charge System, see Figure 1-1).
   c) Maximum power tracking battery charge regulator (Pulse-Width Modulated Transistor Switch used in Adhydrode-Optimum Tracking System, see Figure 1-2).
2. Maximum Power Tracker Circuit.
3. Battery Adhydrode Sense and Control Circuit.
4. Integrated circuits for Ampere-Hour Meter.

The initial effort of the study program was twofold, 1) the adaptation of high efficiency pulse-width (or bucking) regulators and 2) the adaptation of Ampere-Hour Meters to a typical satellite power system.

Since integrated circuits were coming into wide usage, it was decided to design the Ampere-Hour Meter using

integrated circuits. This resulted in some difficulties due to the sensitivity of integrated circuits to power supply and ground line noise. However, a suitable Ampere-Hour Meter was developed that has the following specifications.

Accuracy:	±3% of reading from 10% of full scale to full scale. ±10% of reading from 1% of full scale to 10% of full scale.
Storage:	6 binary bits or 64 states.
Count Direction:	Bi-directional.
Power Drain:	400 MW.
Outputs:	Analog 0-1 V into 1 K. Logical 1 at full charge state. Capable of sequencing the Battery Charge Regulator.
Size (Approx.):	2-1/2 X 2-1/2 X 2 inches
Weight (Approx.):	10 oz.

(An improved version of Ampere-Hour Meter EMAM109 was shipped to NASA Goddard under a separate contract.)

Previously developed bucking regulators were adapted for use as the Load Pulse-Width Regulator and the battery charge regulators. These regulators are characterized by their excellent efficiency (see Figure 4-1). Thus, they have distinct advantages for use in satellite power systems. Very little effort was required to adapt the bucking type of regulator for use as a load regulator. It was necessary, however, to develop various control circuits to make the regulators suitable for use as battery charge regulators. This, also, was successfully accomplished. The specifications for this type of regulator are:

Regulation:	±.5 to ±1% of output voltage for input voltage changes of 2:1 and output load changes of 0 to 100%.
Efficiency:	See Figure 4-1.
Size:	See Figure 4-2.

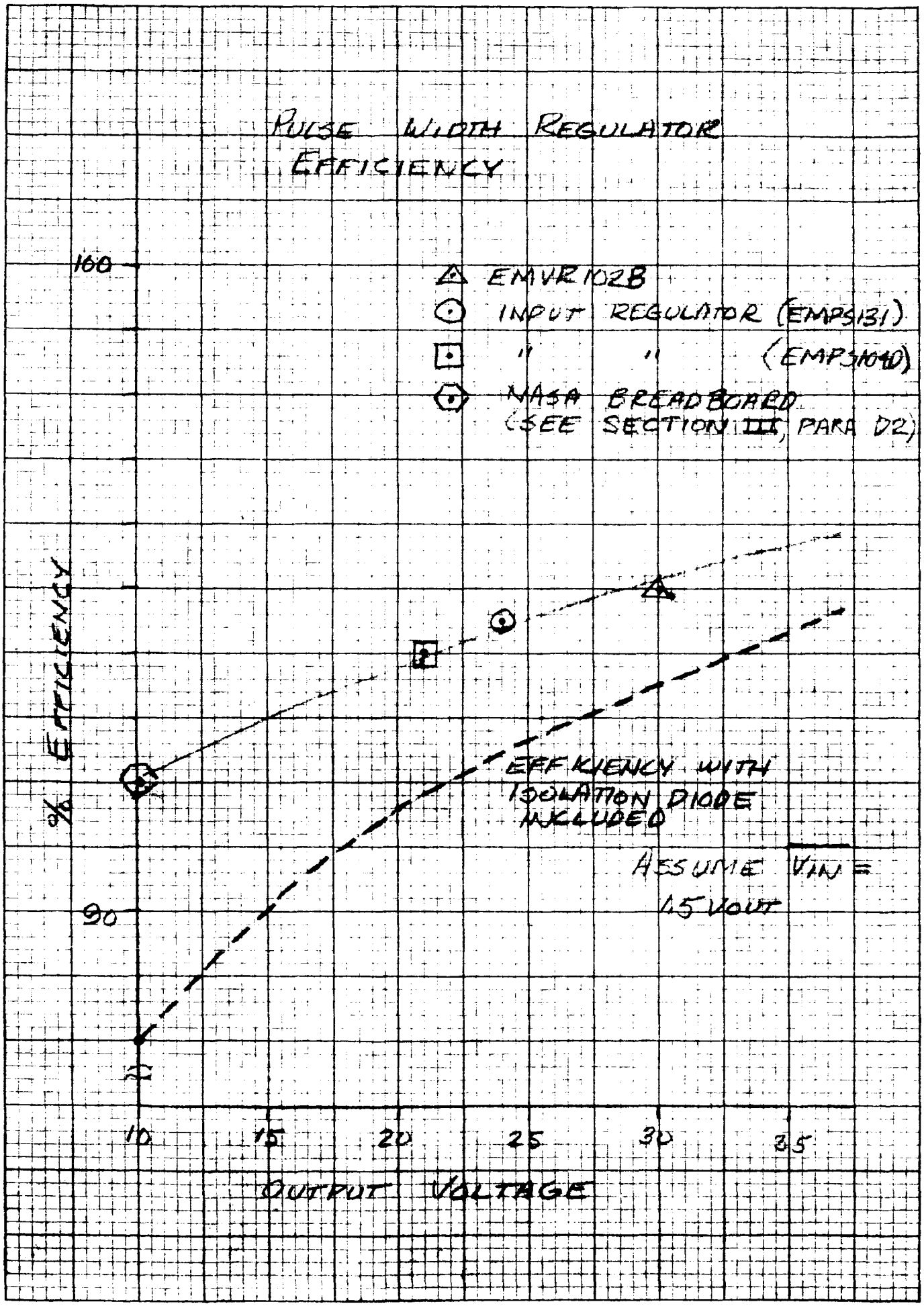


FIGURE 4-1. EFFICIENCY OF REGULATORS
(COMPARISON DATA)

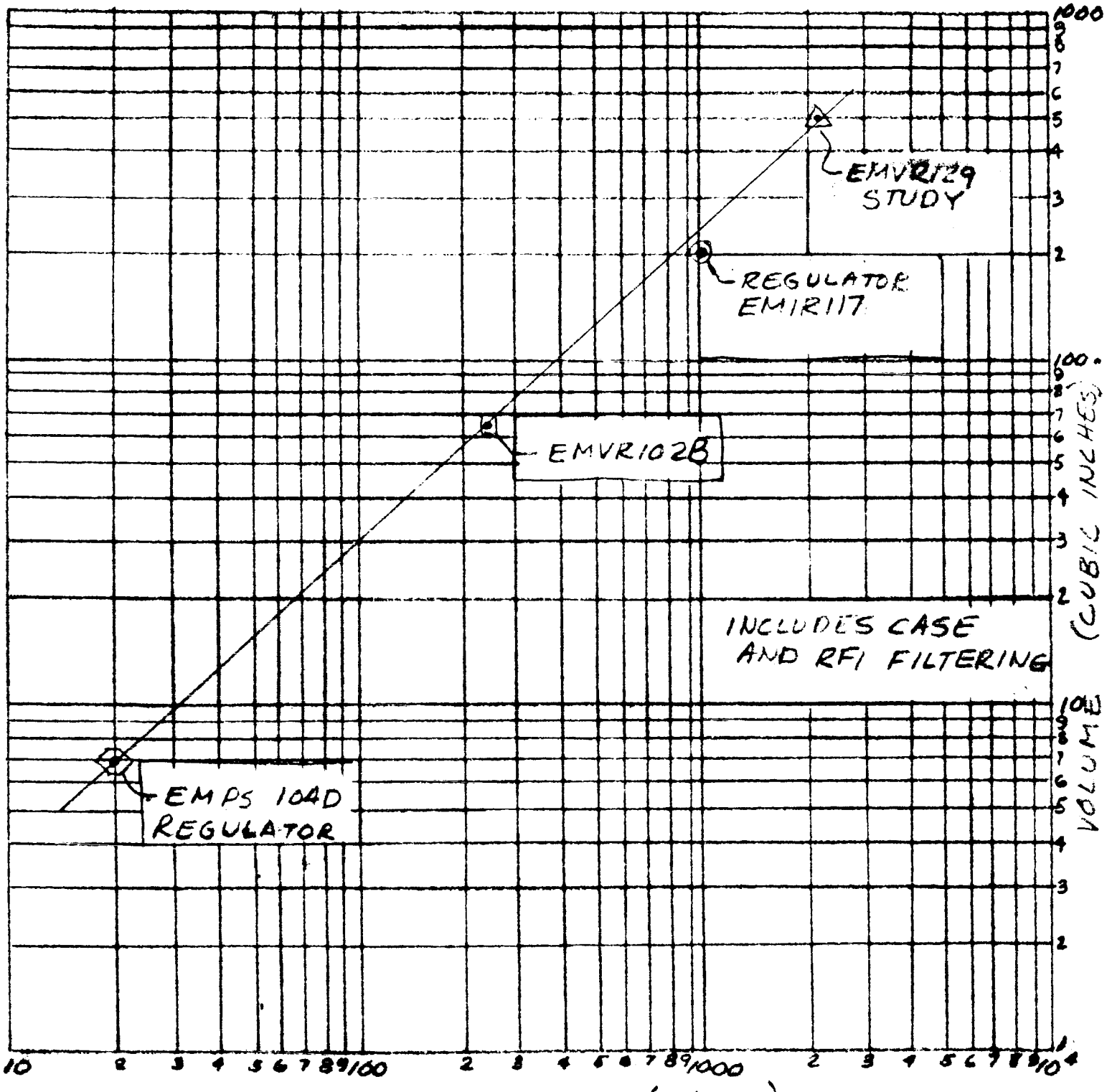


FIGURE 4-2. VOLUME VS. POWER FOR HIGH EFFICIENCY BUCKING REGULATORS

Weight:	See Figure 4-3.
Ripple:	Typically 100 MV.
Output Impedance:	Typically .1Ω at 100 watt power level, inversely proportional to power rating.

Auxiliary Controls:

1. Voltage compensation for battery temperature changes.
2. Switch-to-trickle-charge upon ampere-hour meter or adhydrode sense command.
3. Maximum power matching when operated with Maximum Power Tracker.

During the study program, two other areas seemed worthy of investigation. These were maximum power tracking and adhydrode control of the charger.

Maximum power tracking seemed desirable because of the possibility of matching the solar array to the battery and thus achieving maximum power utilization of the solar array. A simple narrative description of the operation of a power system will show what is meant. Suppose the satellite has just passed from an eclipse into the sunlight. The battery is in its most discharged state (since it has been supplying the satellite load during the eclipse). The solar array is cold and is capable of supplying much more than its normal power (see Figure 4-4). If there was a method to convert this extra power into battery charging current then we could effect the fastest possible recharge cycle. Maximum power tracking provides just such a method for making this conversion. The Maximum Power Tracker adjusts the duty-cycle on the battery charge regulator to match the solar array to the battery. Since the maximum available solar array power is being utilized, it follows that the maximum possible power is flowing into the battery. Further, the battery is very nearly a constant voltage device, thus the maximum possible current is flowing into the battery.

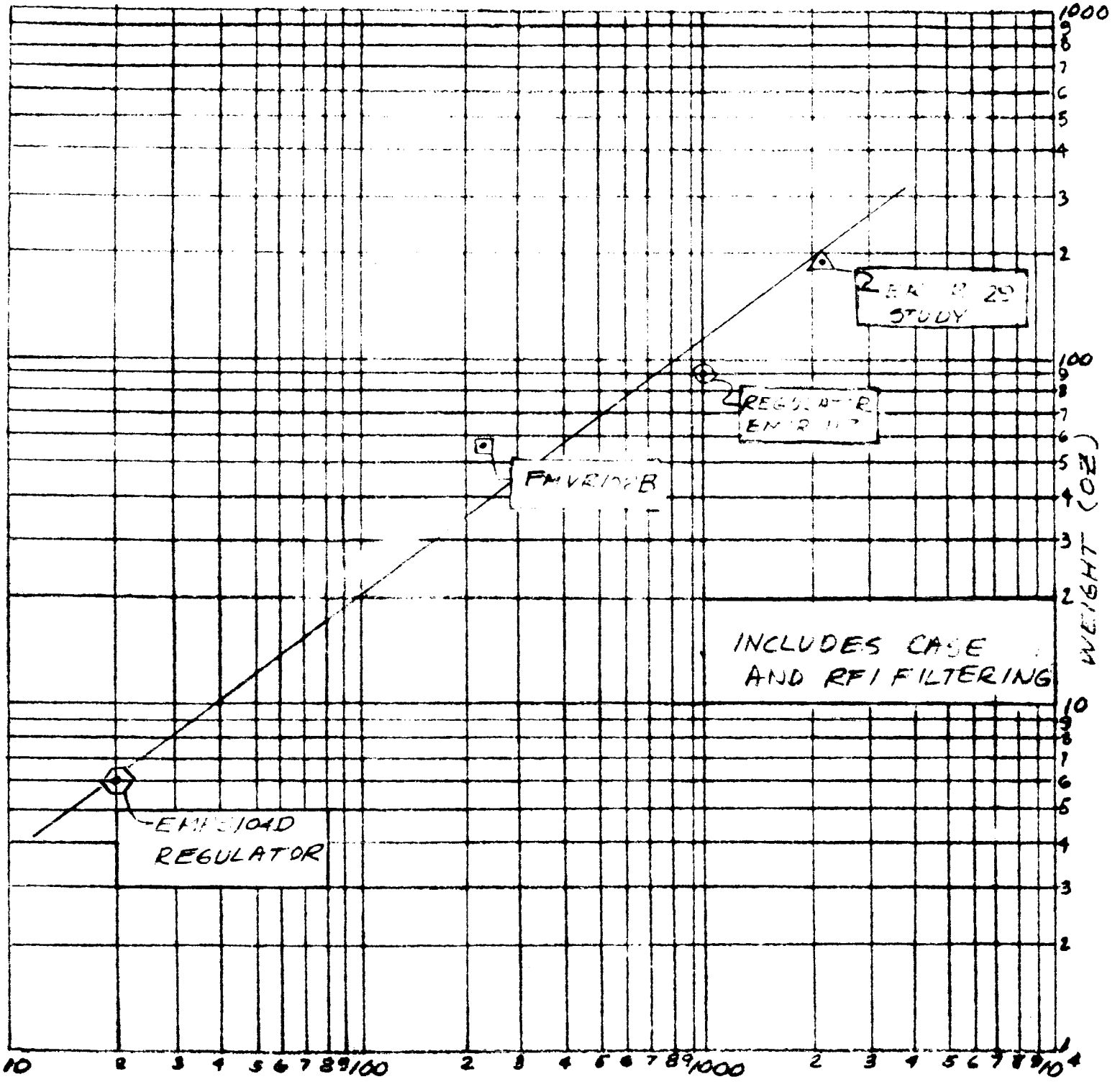


FIGURE 4-3. WEIGHT VS. POWER FOR HIGH EFFICIENCY BUCKING REGULATORS

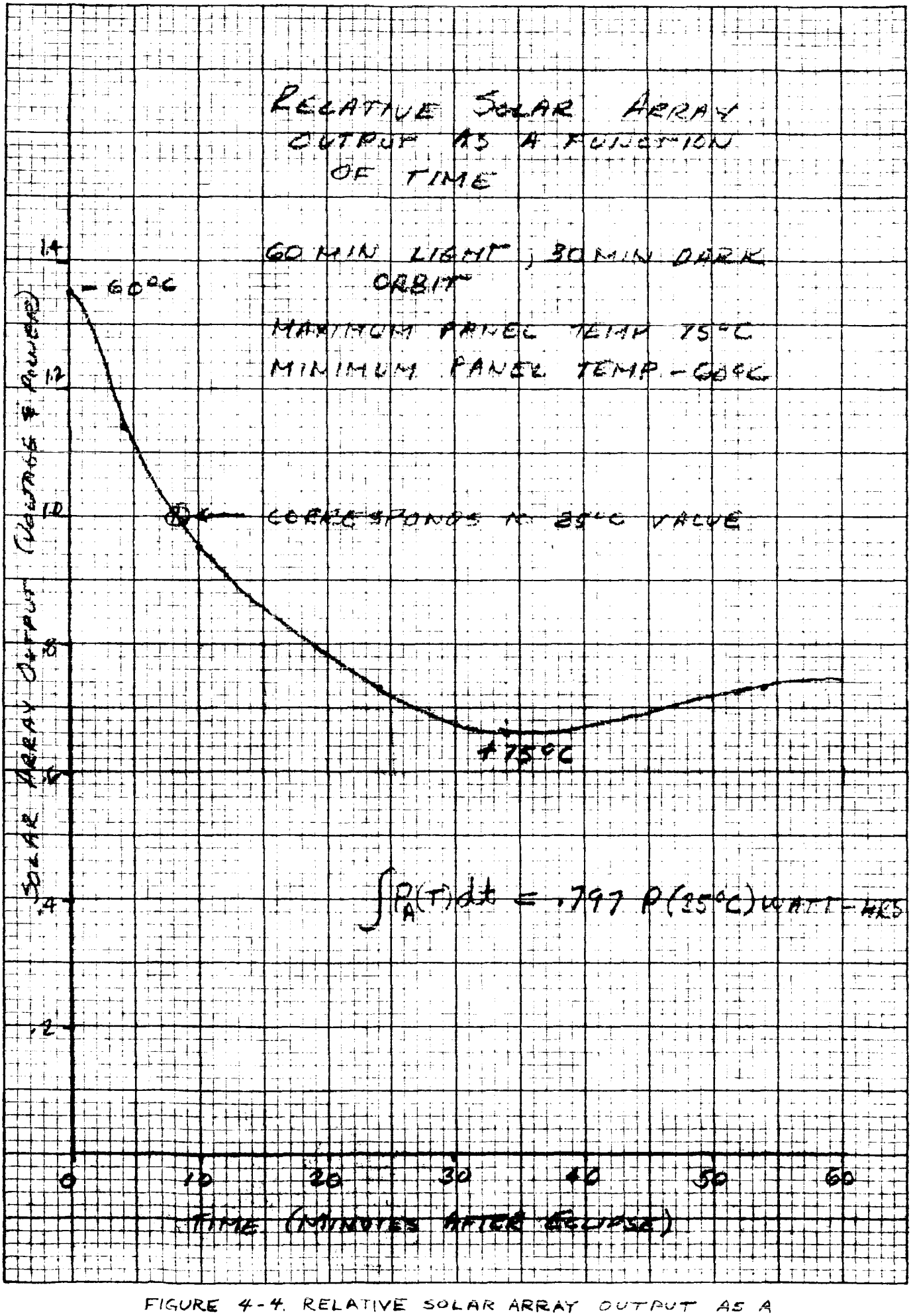


FIGURE 4-4. RELATIVE SOLAR ARRAY OUTPUT AS A FUNCTION OF TIME.

The specifications for the Maximum Power Tracker are:

Accuracy:	See Figure 4-5.
Power Drain:	1.3 watts.
Size (Approx.)	2-1/2 X 2-1/2 X 2 inches
Weight (Approx.)	10 oz.

An Adhydrode Sense and Control Circuit was developed to take advantage of a new development in rechargeable batteries. Battery manufacturers are now able to supply a third electrode (adhydrode) in the nickel-cadmium cells. The adhydrode supplies a signal that is a function of the battery charge state. Thus, it provides an ideal method for charge termination. However, the adhydrode signal level is quite small (typically 20 to 30 MV). A sensor circuit had to be designed and was inserted between the adhydrode(s) and the battery charge regulator. This sensor circuit is the Adhydrode Sense and Control Circuit. The specifications of the Adhydrode Sense and Control Circuit are:

Input:	1 to 4 adhydrodes (temperature compensated).
Output:	Compatible with the battery charge regulator.
Size (Approx.):	2-1/2 X 2-1/2 X 2 inches
Weight (Approx.):	10 oz.

B. ANALYSIS OF A TYPICAL SATELLITE POWER SYSTEM

The following analysis will point out the use of the circuits that were developed, especially the high efficiency buck regulators and the Maximum Power Tracker. A satellite power system can be defined in terms of power distribution as a function of time including power generation, power in loads, and losses.

Let, n = energy efficiency of a power system.

$P_R(t)$ = Regulator power losses as a function of time.

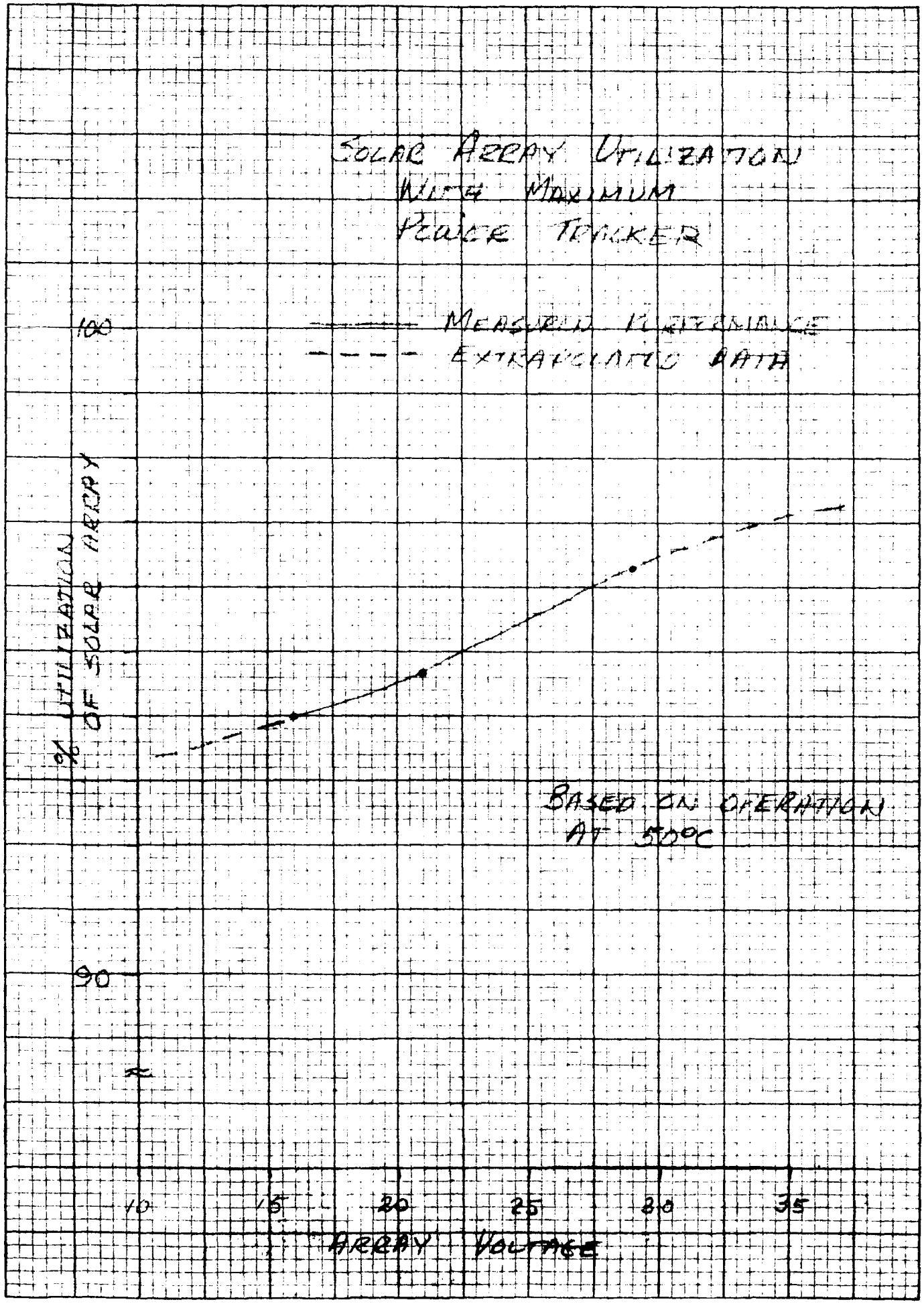


FIGURE 4-5. SOLAR ARRAY UTILIZATION WITH MAXIMUM POWER TRACKER.

$U(t)$ = Utilization as a function of time.

$P_D(t)$ = Isolation diode losses as a function of time.

$P_B(t)$ = Battery losses as a function of time.

$P_A(t)$ = Maximum solar array power as a function of time.

$P_L(t)$ = Load power as a function of time.

$$\int U(t)P_A(t)\,dt = \int P_L(t)\,dt + \int P_R(t)\,dt + \int P_D(t)\,dt + \int P_B(t)\,dt \quad (1)$$

$$n = \frac{\int P_L(t)\,dt}{\int P_A(t)\,dt} \quad (2)$$

This can be related to a typical satellite power system. See Figure 4-6.

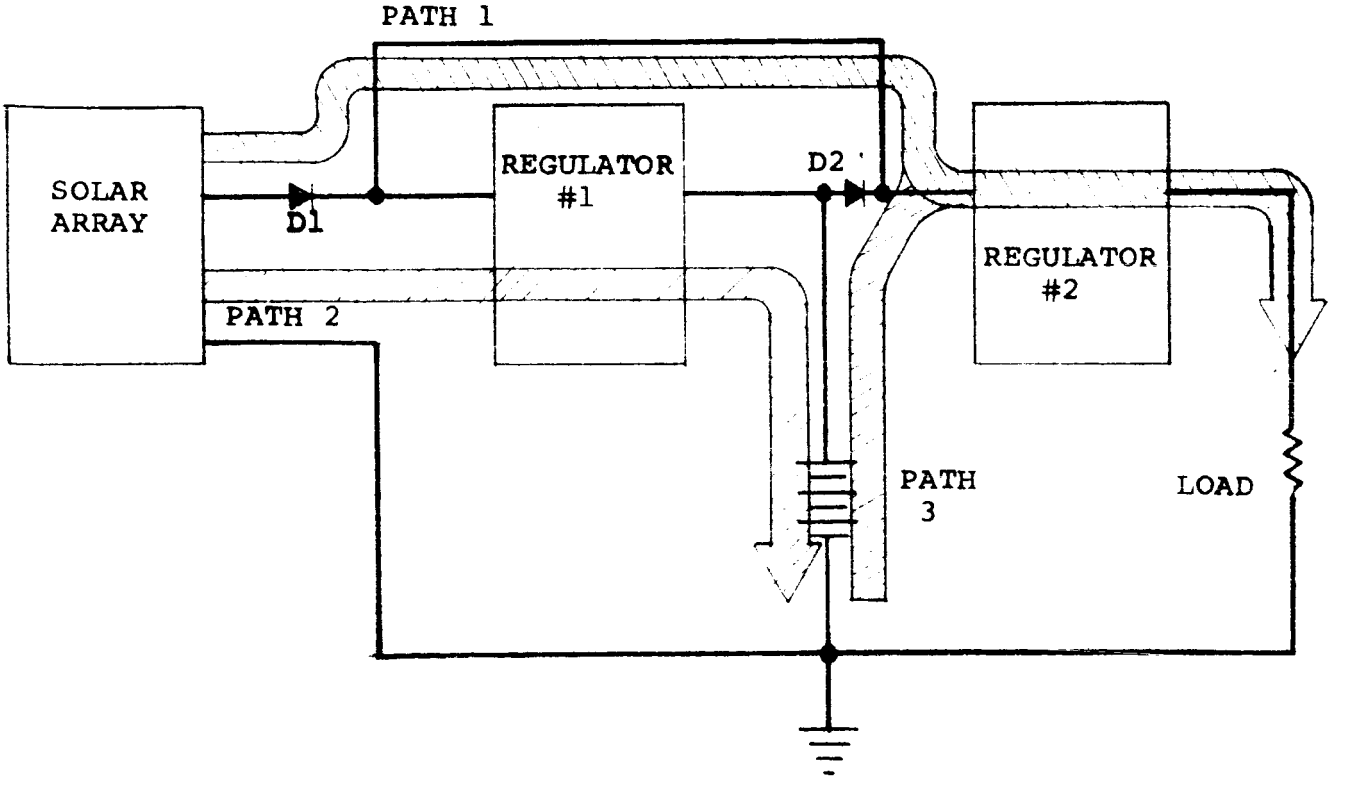


FIGURE 4-6. TYPICAL SATELLITE POWER SYSTEM.

Let, t_L = (%) light period

t_d = (%) dark period

$t_L + t_d = 1$

During the light period (t_L), power flows in paths 1 and 2 of Figure 4-6. During the dark period (t_d), power flows in path 3. Based on Figure 4-6 the various terms in equation (1) can be calculated. Assume that $\int P_L(t)\,dt = 1$, then all calculations are on a per unit basis. The term-by-term calculations are as follows,

$$\int_0^1 P_R(t)\,dt = \int_0^{t_L} P_{R1}(t)\,dt + \int_0^1 P_{R2}(t) \tag{3}$$

The third term of equation (3) is easily calculated since it is $(1-n_R)P_L$, where n_R is the regulator efficiency. If $\int_0^1 P_L(t)\,dt = 1$ and the load is assumed to be constant then P_L is also 1. Hence the third term of equation (3) is $(1-n_R)$. To calculate the first term is more difficult, as it depends on the amount of energy handled by the battery. For the present, let (a) represent a number greater than 1 that accounts for diode losses in D2, regulator losses in Regulator #2, and battery losses. Then, the second term of equation (3) becomes $a(1-n_R)t_L$. Substituting into equation (3),

$$\int_0^1 P_R(t)\,dt = a(1-n_R)t_L + (1-n_R)$$

$$= (1 + at_L)(1-n_R) \tag{4}$$

We can now proceed to the fourth term in equation (1). It can be expressed by,

$$\int_0^1 P_D(t)\,dt = \int_0^{t_L} P_{D1}(t)\,dt + \int_0^1 P_{D2}(t)\,dt. \tag{5}$$

Again, the third term in equation (5) is easily arrived at as in equation (4). The losses in the diode are $(1-n_D)$ where $n_{D_L} = \frac{V_{ARRAY}}{V_{ARRAY} + .7}$ for the period t_L and $n_{D_D} = \frac{V_{BATTERY}}{V_{BATTERY} + .7}$ for the period t_D. Similarly as in equation (4), the second term in equation (5) becomes, $a(1-n_D)t_L$ and here $n_D = \frac{V_{ARRAY}}{V_{ARRAY} + .7}$.

Thus, equation (5) becomes,

$$\int_0^1 P_D(t)\,dt = a\left(1 - \frac{V_A}{V_A + .7}\right) t_L + \left(1 - \frac{V_A}{V_A + .7}\right) t_L + \left(1 - \frac{V_B}{V_B + .7}\right) t_D \qquad (6)$$

Without too great a loss of accuracy, equation (6) can be simplified by using an average voltage throughout and can be called V_{SYSTEM} or V_S. This avoids the problems that would arise if V_{ARRAY} and $V_{BATTERY}$ are functions of time. Then, equation (6) becomes,

$$\int_0^{1,} P_D(t)\,dt = (1 + at_L)\left(1 - \frac{V_S}{V_S + .7}\right) \qquad (7)$$

We come now to the fifth term of equation (1) which is battery losses. We will define another constant (b) which relates to losses in Regulator #2 and losses in diode D2. Then,

$$\int P_B(t)\,dt = b(1-n_B)t_D P_L$$

where n_B = battery efficiency

$P_L = 1$ (by definition)

and $b = \left(\frac{1}{n_R}\right)\left(\frac{V_S + .7}{V_S}\right)$ (8)

Hence,

$$\int P_B(t)\,dt = \left(\frac{1}{n_R}\right)\left(\frac{V_S + .7}{V_S}\right)(1-n_B\ t_D) \tag{9}$$

Calculating (a),

$$a = \underbrace{\left(\frac{1}{n_R}\right)\left(\frac{V_S + .7}{V_S}\right)\left(\frac{1}{n_B}\right)}_{\text{efficiency of path 3}} \overbrace{t_D}^{\text{energy through path 3}} \tag{10}$$

Therefore, equations (4) and (7) become respectively,

$$\int_0^1 P_r(t)\,dt = \left[1 + \left(\frac{1}{n_R}\right)\left(\frac{V_S + .7}{V_S}\right)\left(\frac{1}{n_B}\right) t_L t_D\right]\left[(1-n_R)\right] \tag{11}$$

$$\int_0^1 P_D(t)\,dt = \left[1 + \left(\frac{1}{n_R}\right)\left(\frac{V_S + .7}{V_S}\right)\left(\frac{1}{n_B}\right) t_L t_D\right] \left[1 - \frac{V_S}{V_S + .7}\right] \tag{12}$$

In order to simplify the calculations, assume U(t) equals a constant U. Therefore, equation 2 becomes,

$$n = \left(\frac{\int P_L(t)\,dt}{\int P_L(t)\,dt + \int P_R(t)\,dt + \int P_D(t)\,dt + \int P_B(t)\,dt}\right) U \tag{13}$$

and,

$$n = \frac{U}{1 + \left[1 + \left(\frac{1}{n_R}\right)\left(\frac{V_S + .7}{V_S}\right)\left(\frac{1}{n_B}\right) t_L t_D\right]\left[(1-n_R) \ldots\ldots + \left(1 - \frac{V_S}{V_S + .7}\right)\right] + \left[\left(\frac{1}{n_R}\right)\left(\frac{V_S + .7}{V_S}\right)(1-n_B)(t_D)\right]} \tag{14}$$

C. DESIGN OF A SPECIFIC SATELLITE POWER SYSTEM USING THE TECHNIQUES DEVELOPED

With equation (14), any satellite power system can be analyzed. For example, equation (14) can be used to design a power system with the circuit blocks as developed and having the following requirements:

P_L = 200 watts

V_S = 28 volts

t_D = 33% = 30 minutes

t_L = 67% = 60 minutes

Battery = Nickel-cadmium of appropriate capacity.

From Figure 1, U = .96.

From Figure 4-5, n_R = .94*

From manufacturer's data, n_B = .73**

Substituting into equation (14),

$$n = \frac{.96}{1 + [1 + (1.064)(1.025)(1.37)(.22)]\ [(.06) + (.025)]\ldots \ldots + [(1.064)(1.025)(.27)(.33)]}$$

$$= \frac{.96}{1 + .08 + .033 + .097}$$

Reg. losses — Diode losses — Battery losses

$$= .792$$

The factors in equation (14) may be used to calculate the requirements of the various blocks in Figure 4-6. Obviously, the requirements for Regulator #2 are 200 watts, 20* volts output at 10 amperes load current. The battery watt-hour (WH_B) requirements are:

$$WH_B = P_L \left(\frac{1}{n_R}\right) \frac{V_S + .7}{V_S} t_D$$

$$= 200(1.064)(1.025)(.5)$$

$$= 109.2 \text{ watt-hours}$$

The last number would, of course, have to be corrected for the allowable depth of discharge.

* "Solar Array Battery Power Systems", B. Gladstone

** Page 97 shows why although V_S = 28, V_L = 20V.

Up to this point of the analysis, the type or types of regulators to be used have not been decided. The analysis has been quite general and allows for the use of buck, boost, or buck-boost type regulation. It should be noted that any of these types of regulators are capable of high efficiency power conversion and of performing the matching functions of a maximum power tracking battery charger. However, since the experimental data gathered is based on a bucking type regulator, it is best to finish the design analysis based on the use of bucking type regulators. Using a bucking type regulator for Regulator #2, the minimum battery voltage under discharge must be 20V + 1V (reg. drop) + .7V (diode drop) or 22 volts (at 1V per cell this corresponds to a 22 cell battery. The average voltage for a 22 cell nickel-cadmium battery would be 22 X 1.2 = 26.4 volts. Hence, the average drain would be $200(1.064)(1.025)/26.4 = 8.3$ amps. Thus, the minimum requirement would be 22 cells and 4.15 amp-hours. Since the battery must deliver 109.2 watt-hours and its efficiency is .73, the battery charge regulator must deliver $\frac{109.2}{.73} = 150$ watt-hours. The battery charging voltage will be about 1.45 volts/cell*. Hence, the battery average current is $\frac{150}{1.45 \text{ X } 22} = 4.7$ amps. However, at this point the solar array must be examined. Figure 4-4 shows the output for a typical solar array operating in a 60-30 orbit. Note the output power varies over a range of 2 to 1. Therefore, a 4.7 amp average corresponds to a peak requirement of 10 amps if it is assumed that the bulk of the charging is done early in the light cycle. Thus, the battery

* Value obtained from battery manufacturer's data.

charge regulator is required to deliver 10 amps at 32 VDC.

The solar array requirements can now be calculated. The satellite load will require 218.4 watt-hours while the battery will require (1.064)(1.025)(150 watt-hours) = 164 watt-hours. The utilization is .96. Thus, the solar array must supply 399 watt-hours. Referring to Figure 4-4, this corresponds to a 399/.797 = 500 watt solar array at 25°C.

Due to the use of bucking type regulators for both the Load Pulse Width Regulator and the battery charge regulators, some further constraints on the solar array are necessary. The minimum voltage on the solar array must be greater than the battery charging voltage plus the regulator voltage drop and the diode drop. Thus, $V_{ARRAY(MIN)} = 32 + 1 + .7 \cong 34$ volts. Referring to Figure 4-4, $V_{ARRAY(MIN)}$ occurs at 35 minutes after the eclipse. This voltage is equal to .66 of the 25°C voltage and $\frac{.66}{1.34} = .495$ of the maximum voltage. Hence, the nominal voltage is 51.5 volts and the maximum voltage is 69 volts. The current rating of the solar array can be calculated, which is 500 watts/51.5 volts = 9.7 amps. The satellite power system is now completely analyzed and designed. It is shown in Figure 4-7.

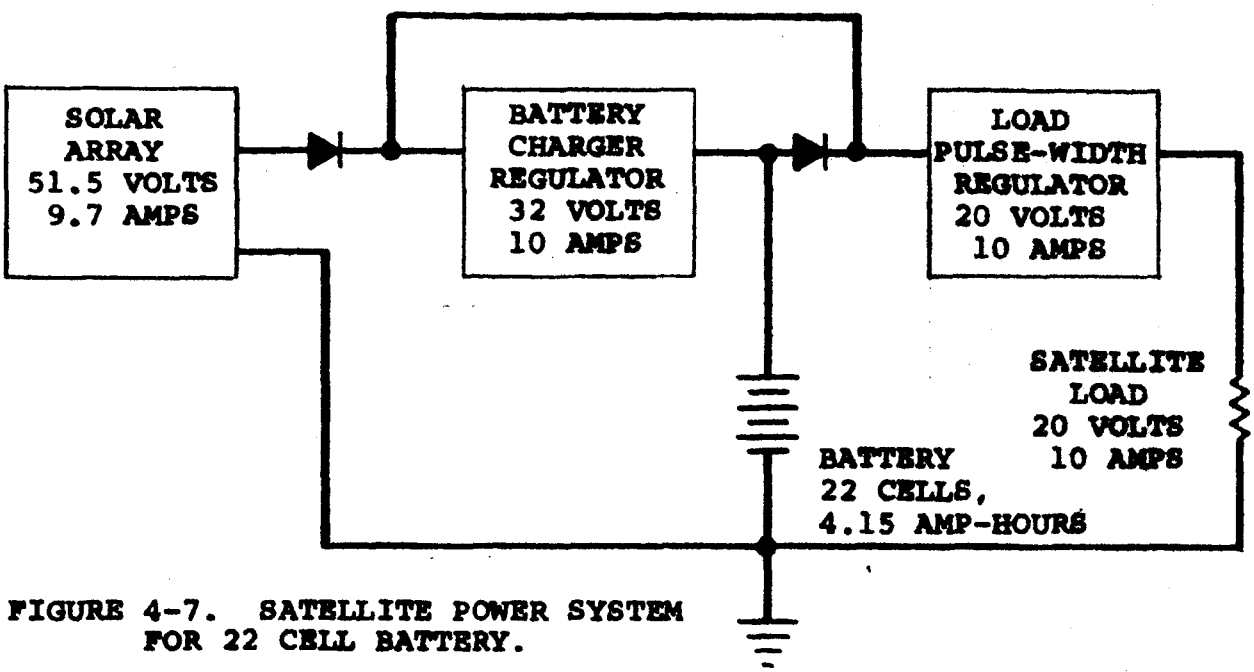


FIGURE 4-7. SATELLITE POWER SYSTEM FOR 22 CELL BATTERY.

Some comments are in order about the satellite power system analyzed in this section. First, note that no safety factor has been designed into the solar array. Any real system would require about 20% safety factor. Second, the battery has been sized for 100% depth-of-discharge which is also unrealistic. Third, note that although the Load Pulse-Width Regulator is 20 volts, the solar array voltage ranges from 34 to 69.5 volts. This means that the Load Pulse-Width Regulator must regulate over a wide range (22 - 69.5V). The average voltage at the input of the Load Pulse-Width Regulator is quite high. Thus the duty cycle is less than 50% most of the time. Both of these conditions are undesirable and tend to reduce the efficiency and increase the size and weight of the Load Pulse-Width Regulator.

By changing the power system somewhat, these conditions can be alleviated. If the Load Pulse-Width Regulator functions as a bucking regulator, then the minimum solar array voltage required to supply the load is

22 volts. In this case the maximum voltage would be 22/.495 or 44.5 volts. In order to charge the battery properly, the charge regulator must be a buck-boost type regulator or the number of cells in the battery should be increased to 31 cells. These alternatives would not really alter the power specifications in the system. A diagram of a satellite power system designed per the last alternative is shown in Figure 4-8.

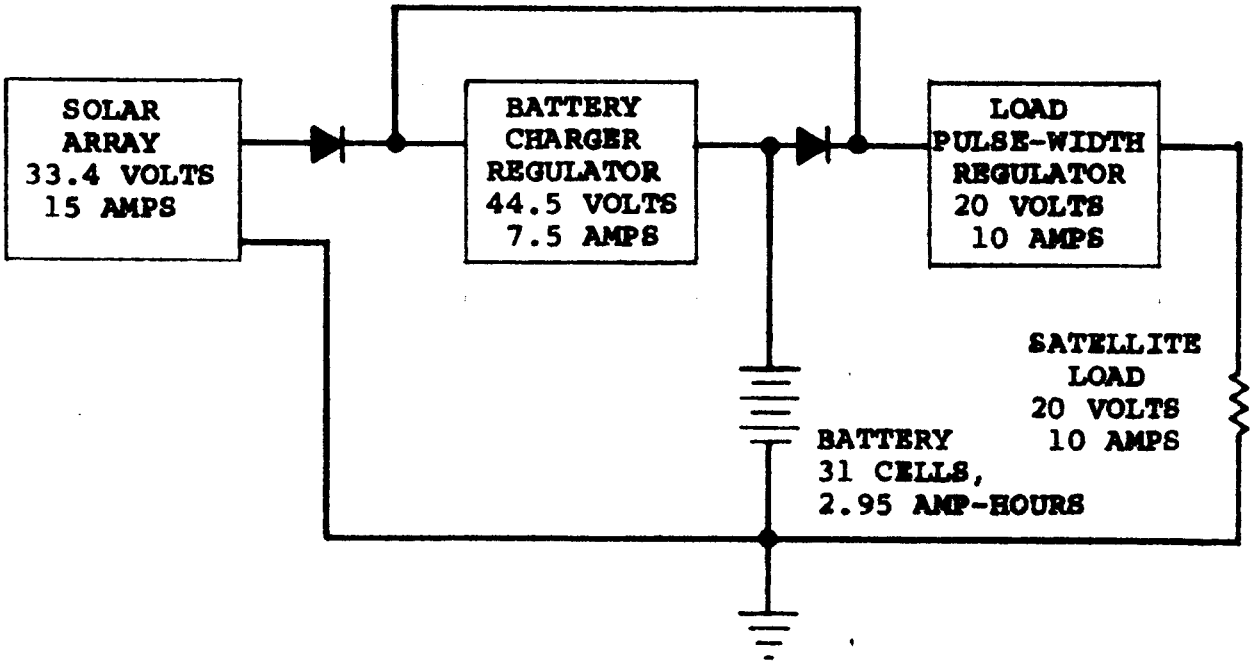


FIGURE 4-8. SATELLITE POWER SYSTEM FOR 31 CELL BATTERY.

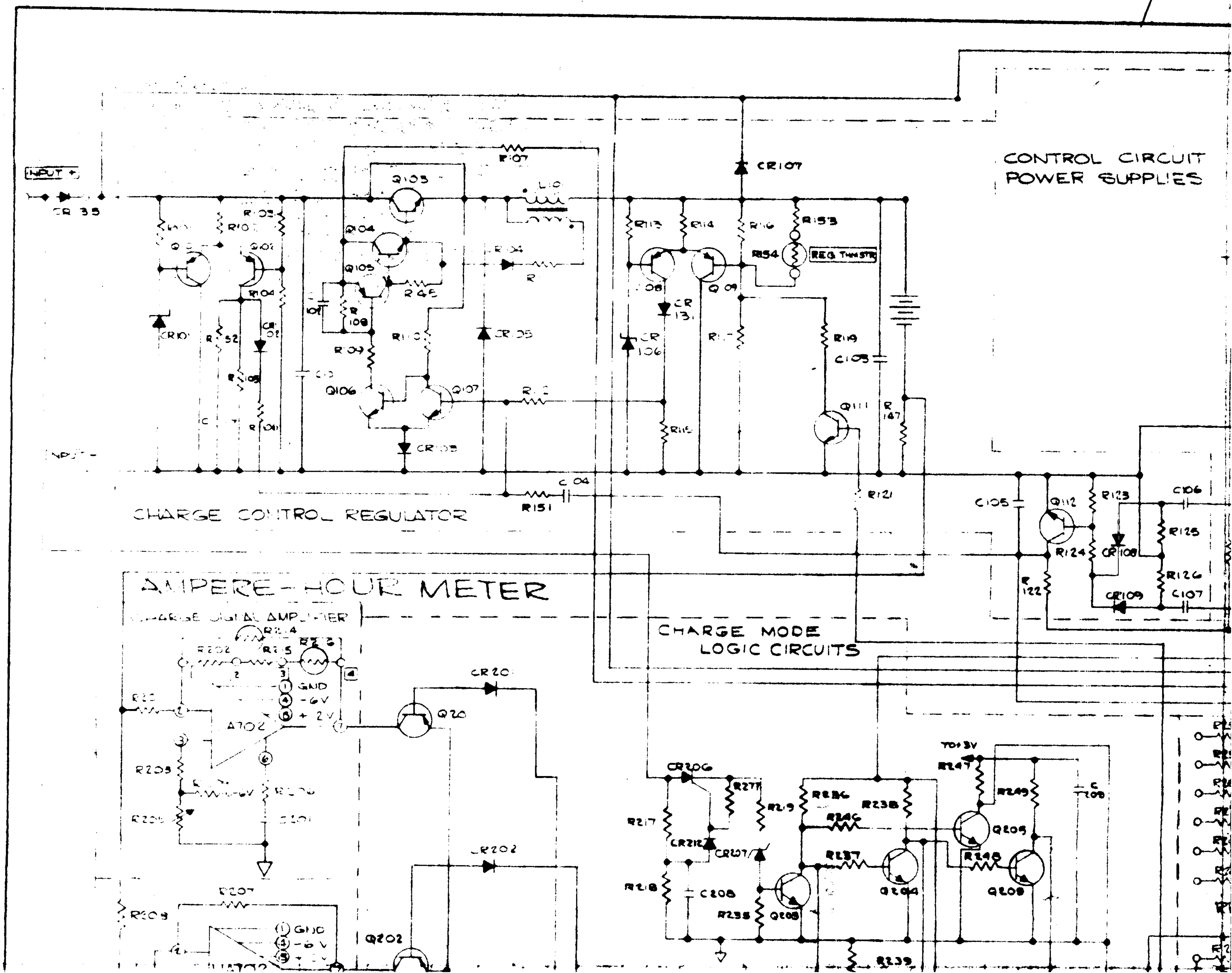
The last example illustrates the flexibility possible in the design of "optimum satellite power systems." It shows that there is no such thing as one optimum power system. There is no real alternative to the careful analysis of power system requirements and thoughtful consideration of alternatives.

A check list of the data required for satellite power system design is;

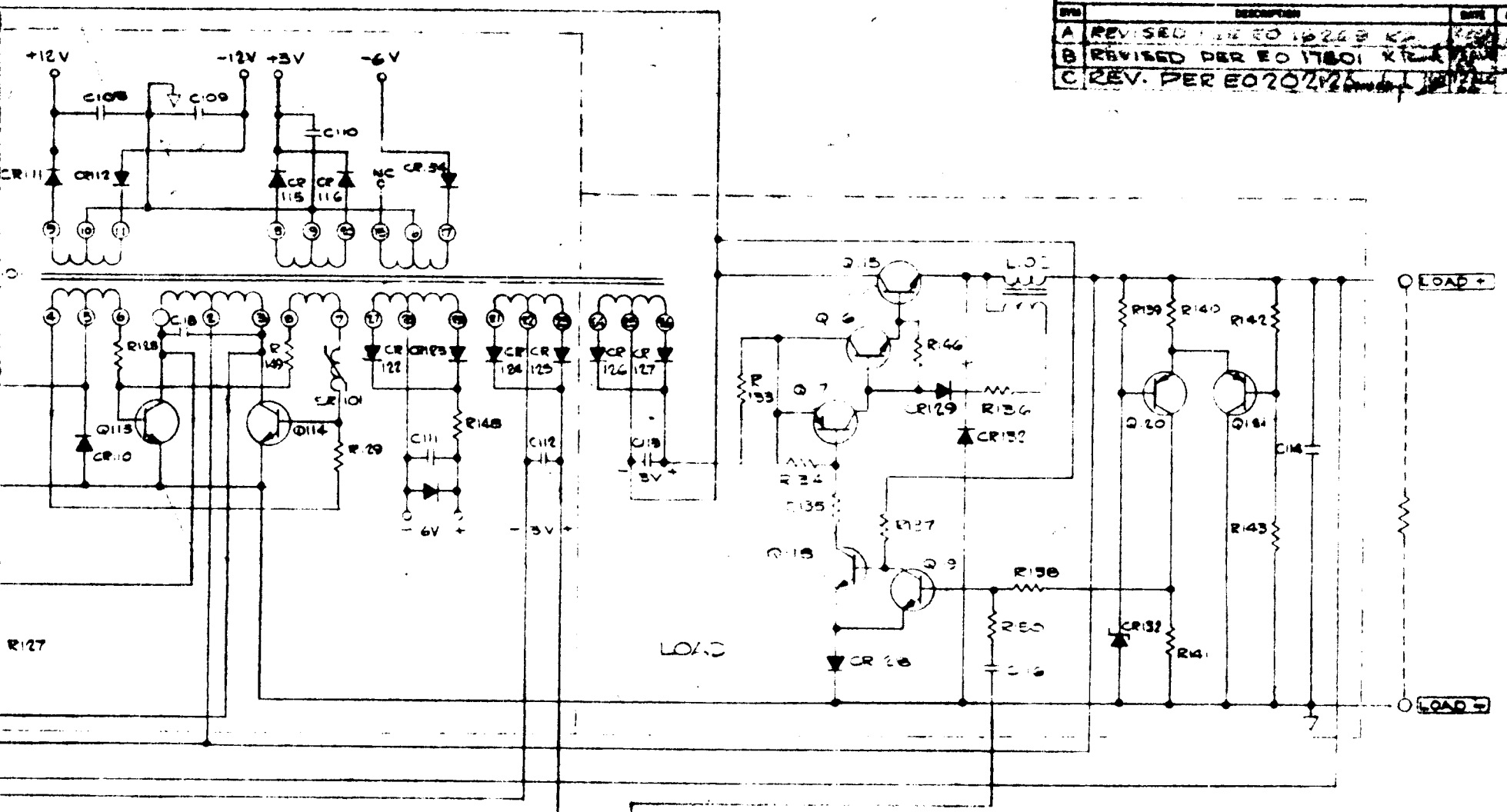
1. Load requirements:
   a. Power, voltages, currents.
   b. Can any loads be time shared.
   c. Peak power demands.
   d. Possible reduced load modes of operation that do not result in failure.
2. Orbit requirements:
   a. Light to dark ratio.
   b. Solar array power variations because of temperature, degradation orientation, etc.
3. Black box specifications:
   a. Efficiency vs. voltage for regulators.
   b. Efficiency of batteries, sizes.
   c. Efficiency vs. power for regulators.
   d. Standby drain of control equipment.
4. Reliability requirements:
   a. Battery depth of discharge.
   b. Possibility of multiple battery-regulator systems allowing partial failures.
   c. Safety factor on solar array.

With this data it is possible to use equation (14) to analyze various combinations to optimize a power system design.

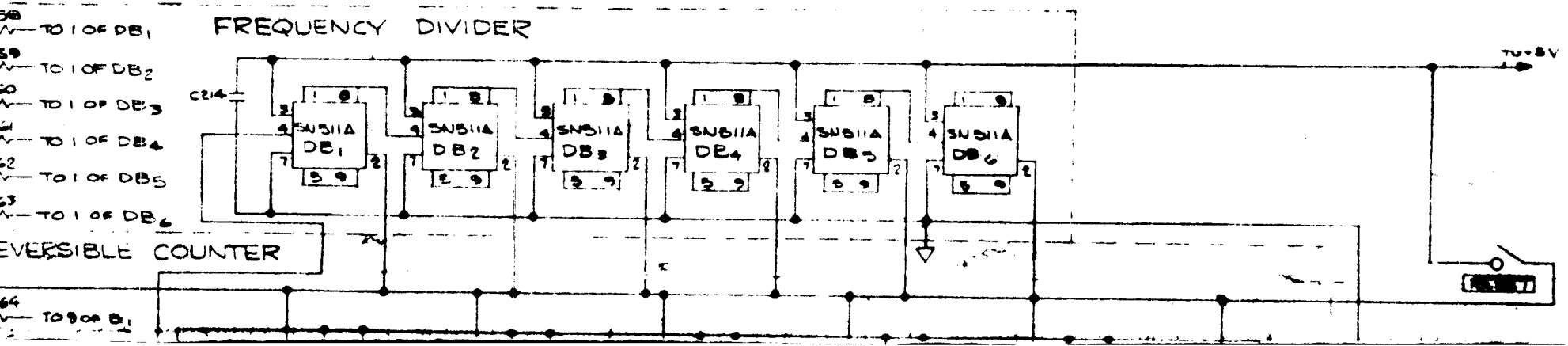
A P P E N D I X

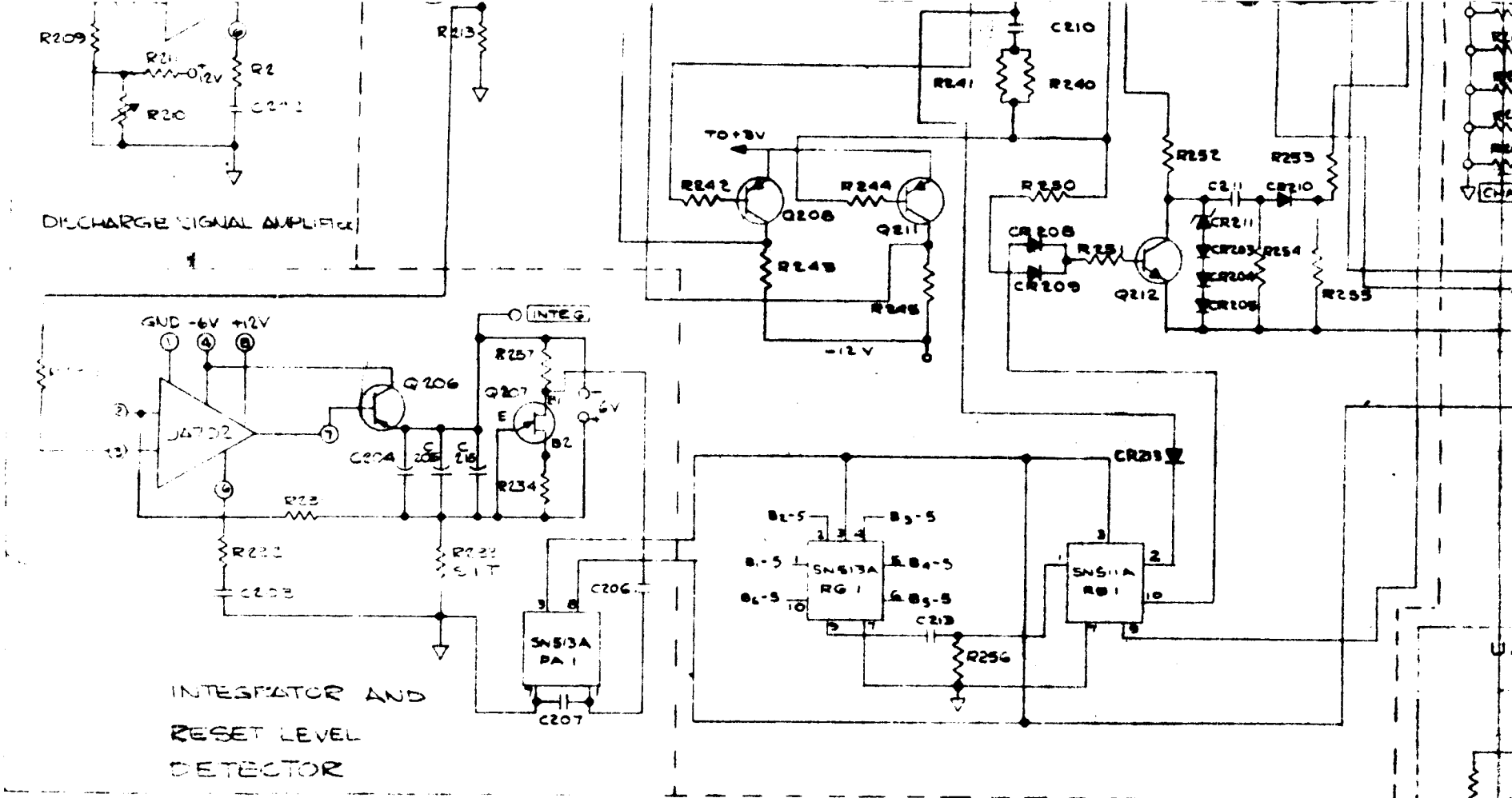

CONTROL CIRCUIT
POWER SUPPLIES
CHARGE MODE
LOGIC CIRCUITS
CHARGE CONTROL REGULATOR
AMPERE-HOUR METER
INPUT +

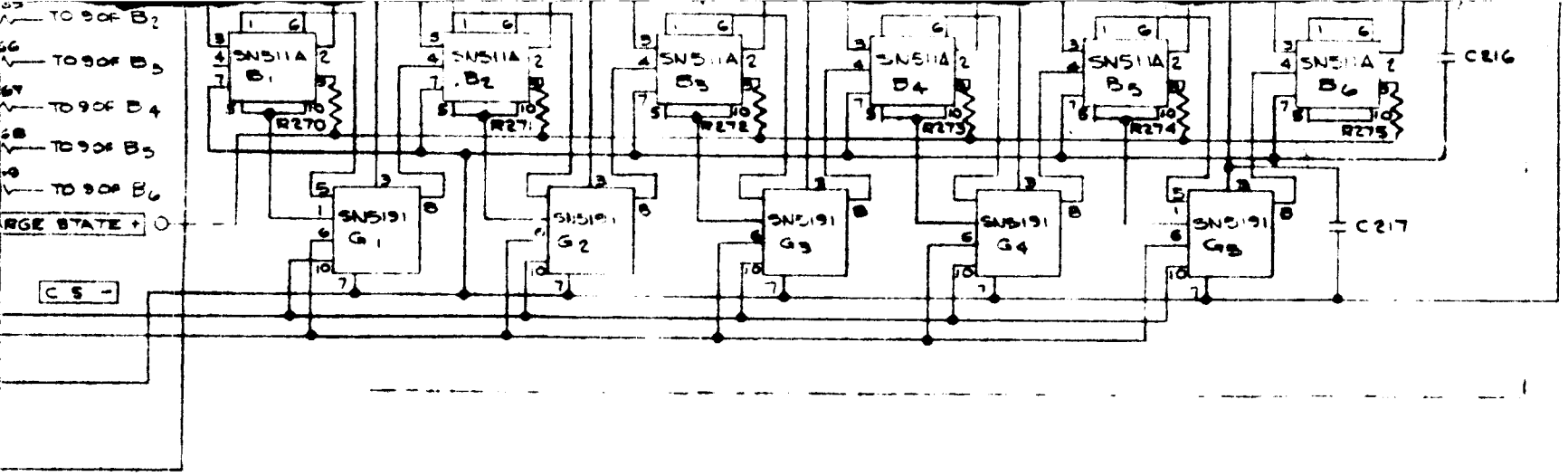
REVISIONS			
DWG	DESCRIPTION	DATE	APPROVED
A	REVISED PER EO 17268 K		
B	REVISED PER EO 17801 K		
C	REV. PER EO 20274		

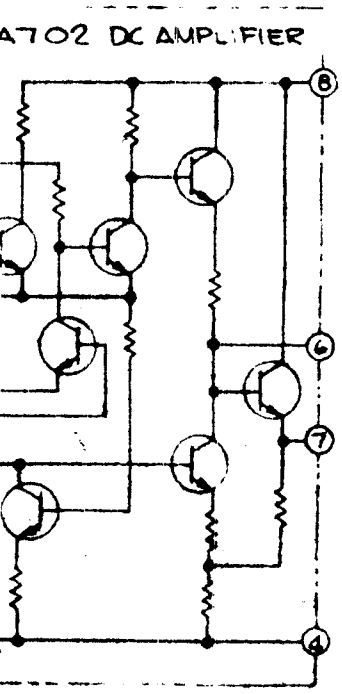


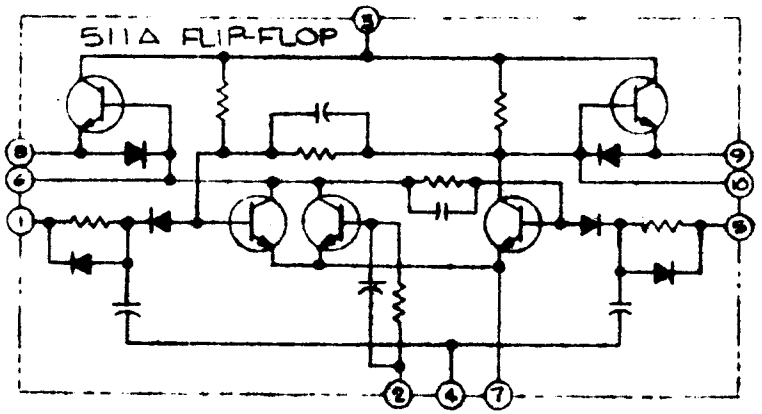
AMPHERE-HOUR METER

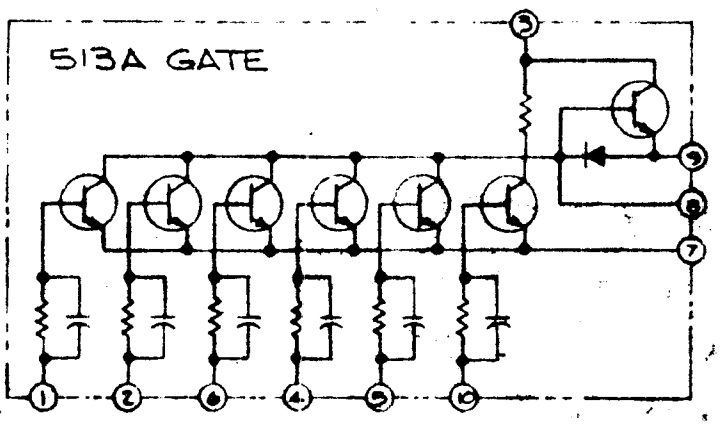












REPORT COPY 1906

QTY REQ'D	PART NUMBER	DESCRIPTION	CODE IDENT	SPECIFICATION	MATERIAL	ITEM NO.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ±1/32 DECIMALS ±.010 ANGLES ±1°
REMOVE SHARP EDGES AND BURRS
MACHINED SURFACES 125

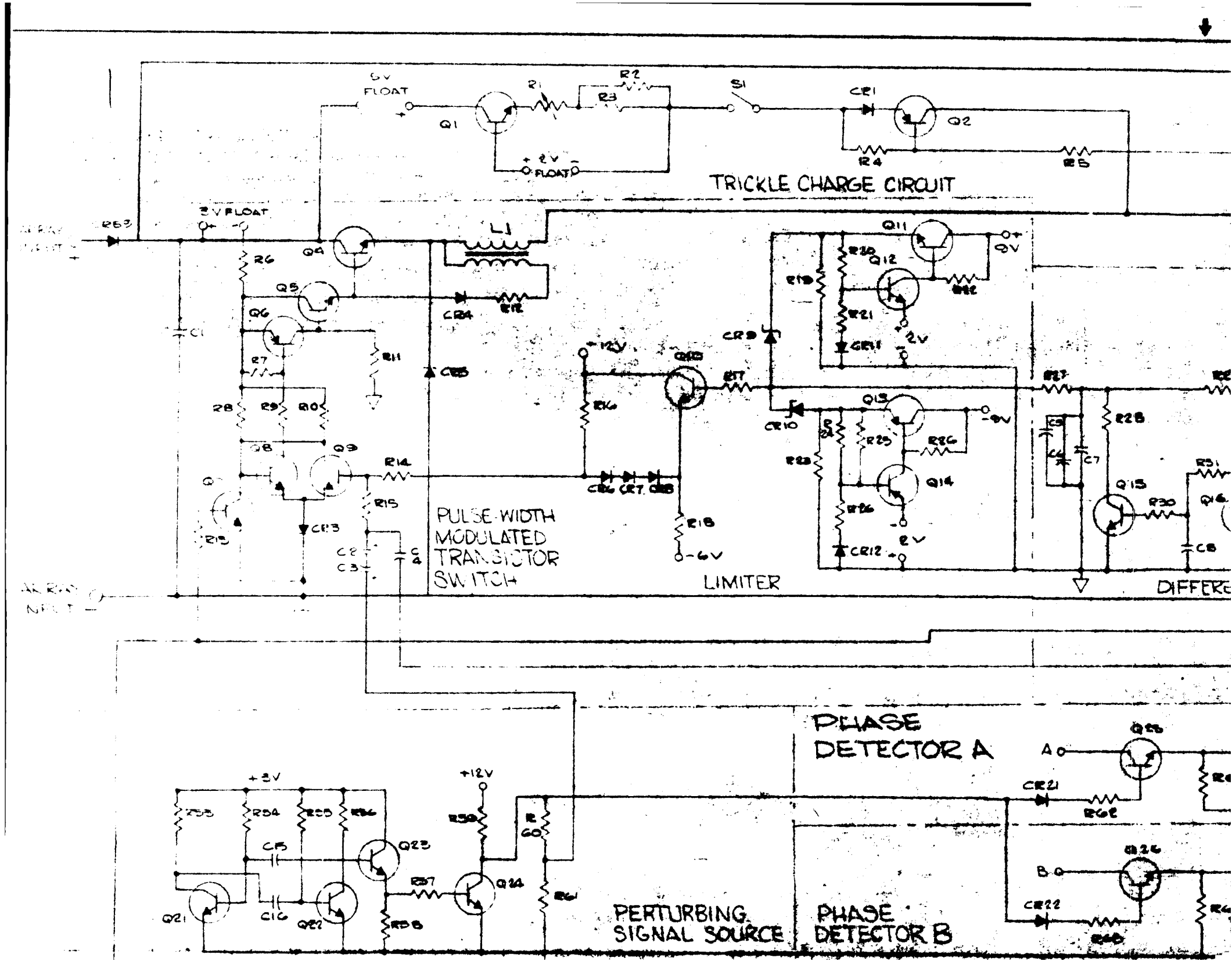
DATE 15 OCT
DR S. L.
CHK
ENGR
MECH ENGR
ELEC ENGR
PROJ ENGR
APPD
APPD

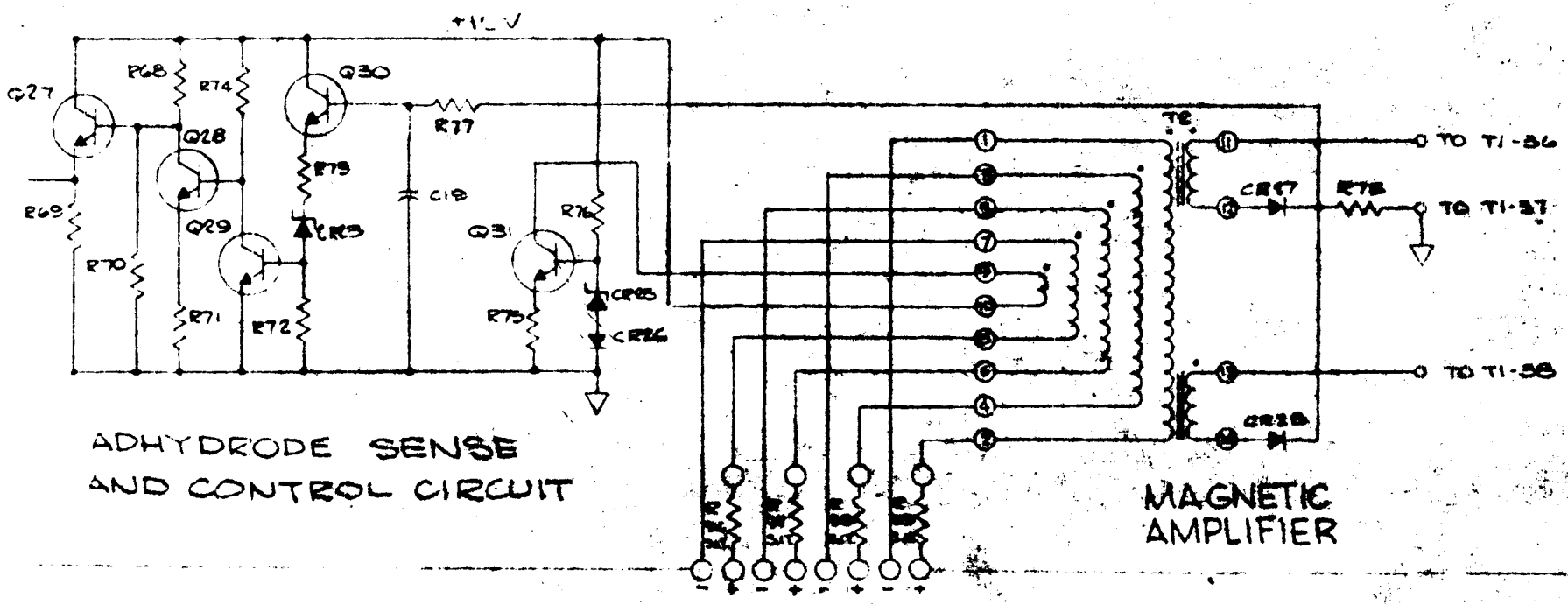
ENGINEERED MAGNETICS

SCHEMATIC DIAGRAM
SATELLITE BATTERY CHARGE
CONTROL SYSTEM BREADBOARD

CODE IDENT NO.	SIZE	DRAWING NO.	REV
06509	E	59055	

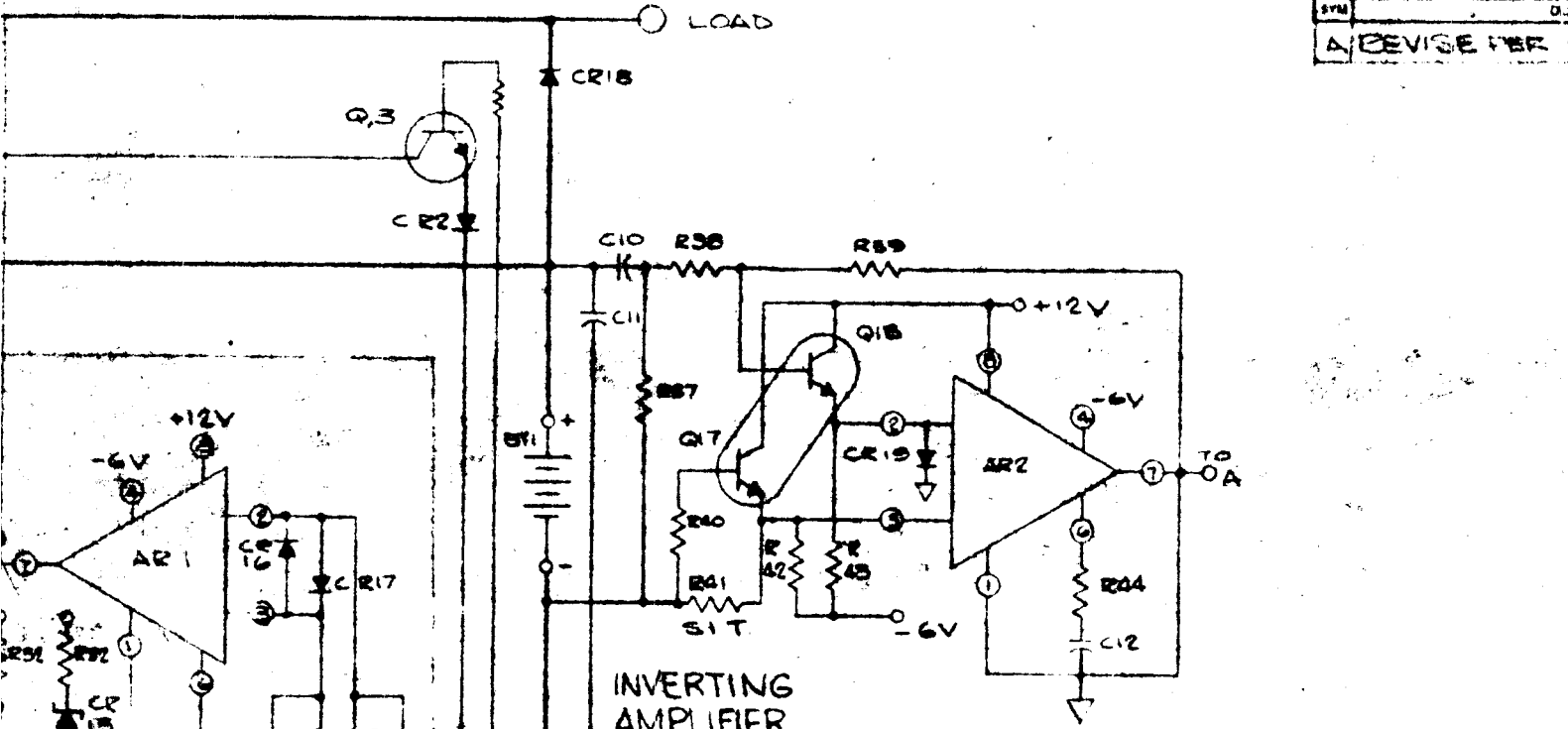
SCALE — SHEET 1 OF 1

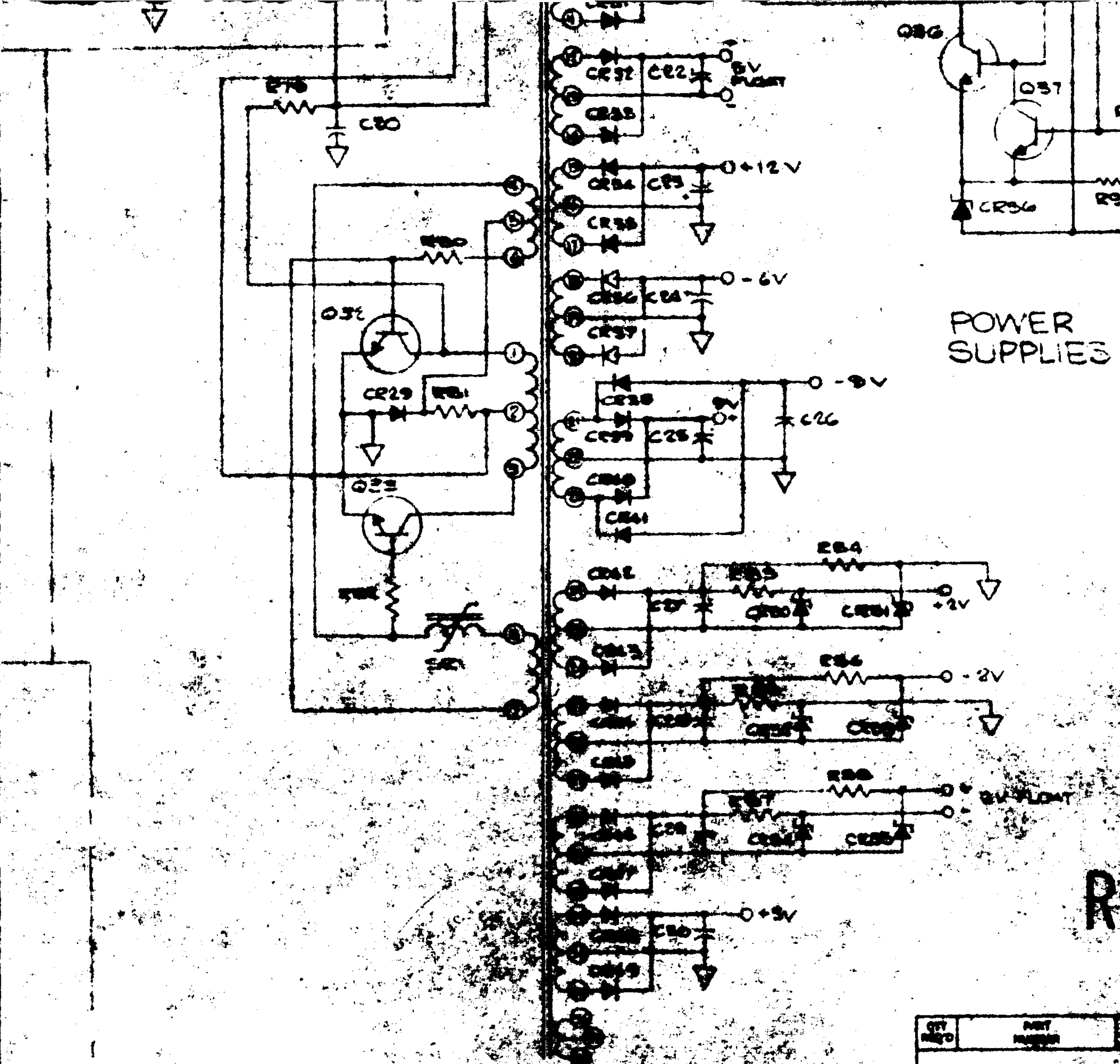

TRICKLE CHARGE CIRCUIT
PULSE-WIDTH MODULATED TRANSISTOR SWITCH
LIMITER
PHASE DETECTOR A
PERTURBING SIGNAL SOURCE
PHASE DETECTOR B



NOTES
1. THE LAST REF DESIGNATIONS USED ARE AR3, ST1, C92, CR55, L1, R88, SE1, T2, Q37
2. UNUSED REF DESIGNATIONS: CR24,58

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	REVISED PER EO 20205		





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QTY REQ'D	PART NUMBER	DESCRIPTION		SPECIFICATION	MATERIAL	ITEM NO.

LIST OF MATERIAL

ENGINEERED MAGNETICS

SCHEMATIC DIAGRAM - SATELLITE BATTERY CHARGE CONTROL SYSTEM BREADBOARD WITH MAXIMUM POWER TRACKER

E 57854 A